

CS 2200 Midterm, Fall 1999
Part A (Closed Book and Notes)
(30 Points, 20 Minutes)

NAME:

NOTE:

- 1. Write your name on every sheet right NOW!**
- 2. Concise bullets are likely to fetch more points than wordy sentences.**
- 3. Legible writing is a requirement not an option!**
- 4. Answer in the space provided.**

1. (1 point) (*Circle one of the following*) The yellow jackets played the following team this past weekend
 - (a) UNC
 - (b) Maryland
 - (c) Army
 - (d) UGA
 - (e) none of a-d
 - (f) How do I know!! I was studying for the midterm!

2. (4 points) Differentiate between *internal* and *external* fragmentation.

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3. (5 points) What are the actions taken by the hardware upon an *interrupt* in a pipelined processor?

4. (5 points) Suggest a scheme to control *thrashing* using the *instantaneous page-fault rate* observed by the operating system.

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5. (5 points) (*Answer True/False with justification*) In an architecture that supports virtual memory, it *always* takes at least 2 trips to the physical memory for every memory access generated by the processor.

6. (5 points) (*Answer True/False with justification*) For a given workload and a given instruction-set architecture, reducing the CPI (clocks per instruction) of all the instructions will *always* improve the performance of the processor.

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7. (5 points) (*Answer True/False with justification*) Having a large register-file is detrimental to the performance of a processor since it results in a large overhead for procedure call/return in high-level languages.

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CS 2200 Midterm, Fall 1999
Part B (Open Book and Notes)
(70 Points, 60 Minutes)

1. (15 points) An architecture has three types of instructions that have the following CPI:

A	2 CPI
B	5 CPI
C	1 CPI

An architect determines that he can reduce the CPI for B to 3, with no change to the CPIs of the other two instruction types, but with an increase in the clock speed of the processor. What is the maximum permissible increase in clock speed that will make this architectural change still worthwhile? Assume that all the workloads that execute on this processor use 30% of A, 10% of B, and 60% of C types of instructions.

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2. (15 points) A memory hierarchy has the following resources:

L1 cache	2 ns access time	98% hit rate
L2 cache	10 ns access time	??
Memory	60 ns access time	

Assume that for each of L1 and L2 caches, a lookup is necessary to determine whether a reference is a hit or miss. What should be the hit rate of L2 cache to ensure that the effective memory access time (P&H book also calls this the Average memory access time) is no more than 3 ns.

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3. (20 points) Consider a pre-emptive priority processor scheduler. There are three processes P1, P2, and P3 in the job mix that have the following characteristics:

Process	Arrival time	Priority	Activity
P1	0 sec	1	8 sec CPU burst followed by 4 sec I/O burst followed by 6 sec CPU burst and quit
P2	2 sec	3	64 sec CPU burst and quit
P3	4 sec	2	2 sec CPU burst followed by 2 sec I/O burst followed by 2 sec CPU burst followed by 2 sec I/O burst followed by 2 sec CPU burst followed by 2 sec I/O burst followed by 2 sec CPU burst and quit

What is the *turnaround time* for each of P1, P2, and P3? What is the *average waiting time* for this job mix?

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4. (20 points) Consider an architecture wherein for *each entry* in the TLB there is 1 reference bit (that is set by hardware when the associated TLB entry is referenced by the CPU for address translation), and 1 dirty bit (that is set by hardware when the associated TLB entry is referenced by the CPU for a store access). These bits are in addition to the other fields of the TLB that we have discussed in the class. The architecture provides *three* special instructions: one for sampling the reference bit for a particular TLB entry (*Sample_TLB(entry_num)*); one for clearing the reference bit for a particular TLB entry (*Clear_refbit_TLB(entry_num)*); and one for clearing the reference bits in all the TLB entries (*Clear_all_refbits_TLB()*). Come up with a scheme to implement page replacement using this additional help from the TLB. For full credit, you should show data structures and pseudo code that the algorithm maintains to implement page replacement. Use back of the page if necessary.