

# GEORGIA INSTITUTE OF TECHNOLOGY

College of Computing

## CS6290/CS4290 — High-Performance Computer Architecture

Fall 2000

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CS6290/CS4290  
Homework 1

Issued: August 25, 2000  
Due: September 1, 2000

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**Purpose:** This homework covers Amdahl's law, instruction sets and some VLSI issues.

**Reading:** H&P Chapters 1, 2 for background.  
[Patterson85] to be discussed in class Friday.

**Problems:**

1. Performance and Amdahl's law.
2. Instruction sets.
3. VLSI and technology limits.
4. Read [Patterson85].

**Collaboration:** (*As in the syllabus*) collaboration on projects and homework in **pairs** is encouraged. If you work in a pair, turn in one write-up with the names of both collaborators. You're welcome to discuss high-level concepts with other groups, but all homework solutions must be worked out and written up separately.

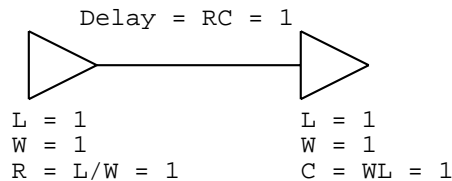
**Problem 1:** Amdahl's Law

- A:** Problem 1.2 in the book.
- B:** Problem 1.12 in the book.

**Problem 2:** Instruction Sets

- A:** Problem 2.3 in the book. Show all four code sequences as well as the computed code sizes and total memory bandwidths. The four variables should start and end in memory.

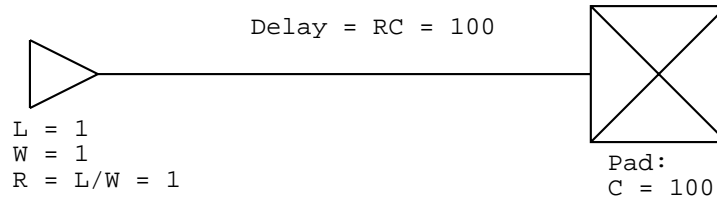
**Problem 3:** VLSI and Technology Limits



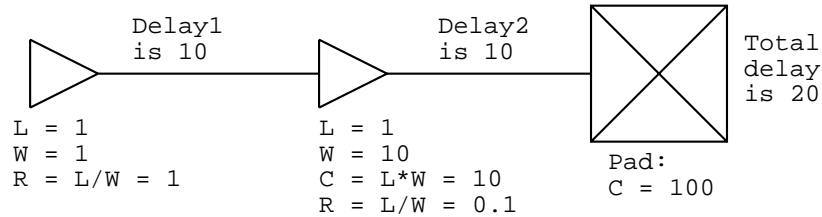
**Figure 1:** Minimum-size gate driving a minimum-size gate. The delay is  $1\tau$ , where  $\tau = R_{min} \cdot C_{min}$ .

A unit-size buffer is made of minimum size (length 1, width 1) transistors. Assume that a unit-size buffer has an ON-resistance of 1 (actually  $1 \cdot R_{min}$  Ohms but we'll drop the units) and a gate capacitance of 1 ( $1 \cdot C_{min}$  Farads). If a unit-size buffer drives another unit-size buffer (Figure 1), the gate delay of the first is then  $1 \cdot 1 = 1$  (with units:  $R_{min} \cdot C_{min} = 1 \cdot \tau$  Seconds). Note that if a unit-size gate drives a double-size gate the delay doubles. If a double-width gate drives a unit-size gate, the delay halves.

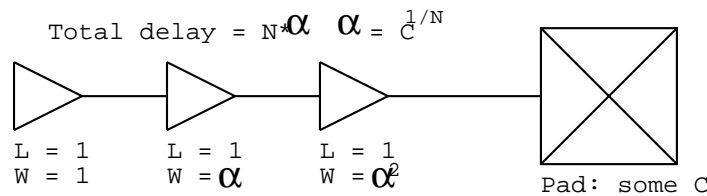
When driving a large capacitive load (say a pad with a capacitance of 100 times that of a minimum-size buffer), from a unit-sized buffer (Figure 2, next page), it is faster to add additional buffers of increasing size between the unit-sized buffer and the large load. For instance, Figure 3 shows a two-stage driver and Figure 4 shows an  $N$ -stage driver where each stage is  $\alpha$  times larger than the previous stage.



**Figure 2:** Minimum-size gate driving a pad with a capacitance of  $100 \cdot C_{min}$ . The resulting delay is  $100 \cdot \tau$ .



**Figure 3:** Here's a two-stage string driving the same pad. The middle buffer in the string is sized  $10 \times$  wider than minimum giving it  $10 \times$  the capacitance but also  $0.1 \times$  the resistance of a minimum-size device. The total delay is thus  $20 \cdot \tau$ .



**Figure 4:**  $N$ -stage string scaled up by a factor of  $\alpha$  per stage. The total delay is  $N \cdot \alpha \cdot \tau$ . The scaling factor,  $\alpha$ , is the  $N$ th root of the total load to be driven.

**A:** As mentioned in class, the *optimal* solution is to size the buffers so that  $\alpha = e$  ( $e$  as in the base of natural logarithms) and to use as many buffers in the string as needed. **Prove** that this solution is optimal. Feel free to treat  $N$ , the number of buffers, as a fraction for the purposes of a solution.

**Problem 4: Reading**

(0 points) Please read [Patterson85] in order to be prepared to discuss it on Friday, September 1st, the day this problem set is due.