

# GEORGIA INSTITUTE OF TECHNOLOGY

College of Computing

## CS6290/CS4290 — High-Performance Computer Architecture Fall 2000

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CS6290/CS4290  
Homework 3

Issued: September 22, 2000  
Due: September 29, 2000

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**Purpose:** This homework reviews pipeline operation and instruction-level parallelism.

**Reading:** H&P Chapter 3 for background.  
[Fisher91]

### Problem 1: Pipeline Operation

**A:** Problem 3.1 in the book.

### Problem 2: Reading

[Fisher91] Joseph A. Fisher and B. Ramakrishna Rau, “Instruction-Level Parallel Processing”, *Science*, 253, pages 1233-1241, September 13, 1991.

**A:** Read [Fisher91] above and write a one paragraph summary of the key *compiler* techniques that enable instruction-level parallelism. Note, one paragraph means something like 4-5 sentences on a third of a page.