

GEORGIA INSTITUTE OF TECHNOLOGY

College of Computing

CS6290/CS4290 — High-Performance Computer Architecture

Fall 2001

CS6290/CS4290

Homework 5

Issued: October 19, 2001

Due: October 26, 2001

Purpose: This homework covers prediction.

Reading: H&P Sections 4.3, 4.6
[Emer97]

Problems:

1. Mispredict Penalty.
2. Predictor Circuits.

Collaboration: (*As in the syllabus*) collaboration on projects and homework in **pairs** is encouraged. If you work in a pair, turn in one write-up with the names of both collaborators. You're welcome to discuss high-level concepts with other groups, but all homework solutions must be worked out and written up separately.

Problem 1: Mispredict Penalty

A: Problem 4.10 in the book.

Problem 2: Prediction Circuit

Here's a predictor described using the notation from [Emer97]. I've extended the notation slightly with a `define` keyword meant to distinguish between definitions and instances: a definition just describes how to build a structure. An instance is the real structure.

The variables `PC`, `DIR` and `TAKEN` come from the processor state: the program counter, the direction of the branch instruction (forwards or backwards) and whether the branch was ultimately taken or not.

```
/*
 * first, a familiar definition: an N-bit predictor array.
 * The 'P' inside the definition refers to the results of the
 * prediction. The ++ and -- operators above are defined to be
 * saturating arithmetic with nbits of precision.
 */
define nbit[nbits, depth](index, feedback)
    = MSB(P[nbits, depth](index, (MSB(P) == T) ? P++ : P--));

/*
 * second, three 'mystery' definitions of structures.
 */
define foo[](index, feedback)
    = P[1, 256](index, feedback);
define bar[](VOID, feedback)
    = P[8, 1](0, (P << 1) | feedback);
define baz[](index, feedback)
    = P[8, 256](index, (P << 1) | feedback);

/*
 * third, the actual instance of the predictor. It includes instances
 * of all the definitions above.
 */
prediction = nbit[3, 256]((PC
                        xor bar[](VOID, TAKEN)
                        xor baz[]((PC << 1) | foo[](PC, DIR), TAKEN)),
                        TAKEN);
```

A: Draw and label the circuit described by the notation above. Label all storage arrays with sizes and all wires with widths.

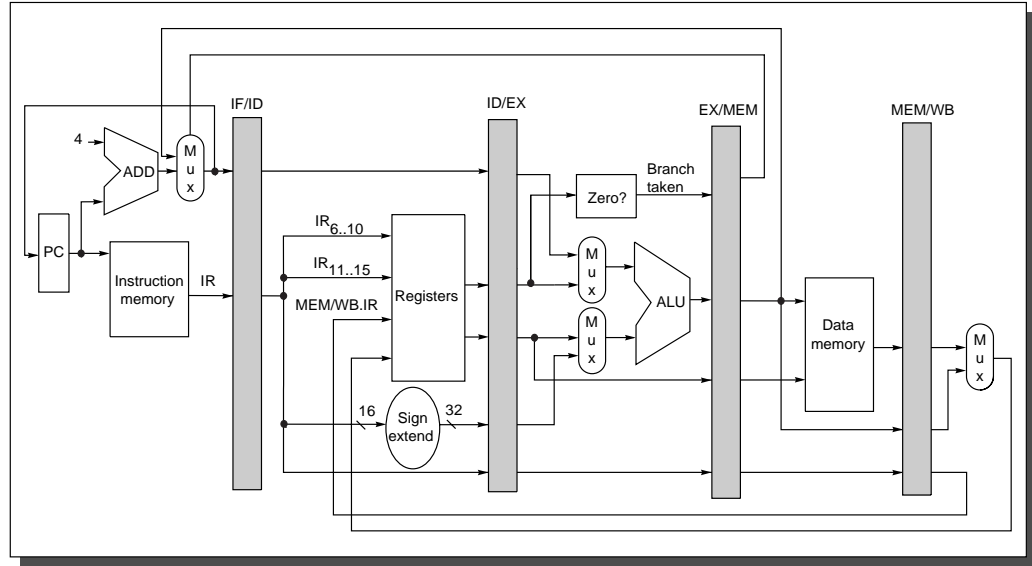


FIGURE 3.4 The datapath is pipelined by adding a set of registers, one between each pair of pipe stages.

B: Referring to Figure 3.4 in the text (reproduced above), where do the PC, DIR and TAKEN signals come from? Indicate with wires drawn on the diagram. Copies of the diagram are available online if useful.

C: What does the `foo[]` structure do in the in predictor? Why is it needed?

D: What information does the `bar[]` structure provide in the predictor?

E: What information does the `baz[]` structure provide in the predictor?