

Homework 3 (due 3/13/2002)

We have discussed two-phase locking several times throughout the semester. Show the code (at the level of the code in the “Spinlocks for SMPs” slides) for two phase spin-locking. That is, consider a critical section with two locks (`lock1` and `lock2`) which can be acquired in any order. Design a spin-lock that satisfies the following requirements:

- Deadlock is prevented (i.e., it is never the case that a holder of `lock1` is waiting for `lock2` while a holder of `lock2` is waiting for `lock1`).
- The lock has good performance in terms of latency, delay, and bandwidth consumption on an SMP machine with snooping caches.

You can assume that the contention for locks is low (a well designed concurrent program typically will not have high contention)—that is, there are very rarely more than 2 threads spinning.

Justify with a couple of sentences why your lock works well.