

Wednesday, April 17 2002

Tips on project presentations with powerpoint slide show.

Documentation: /net/hp82/softarch/DOCS/

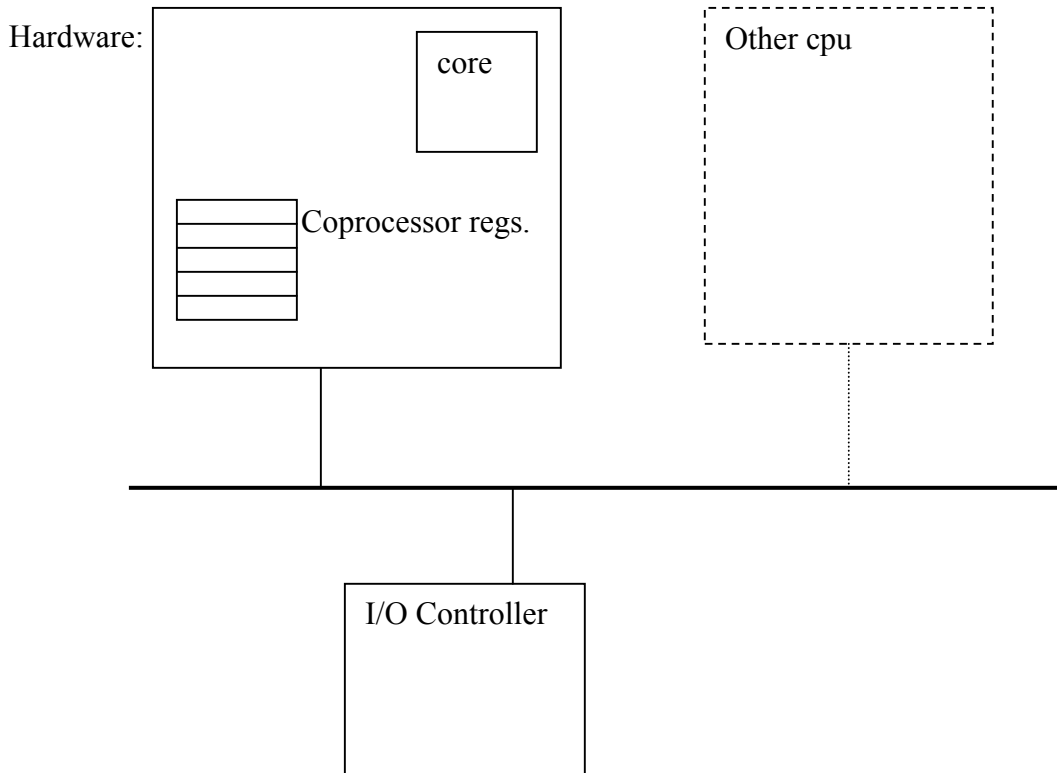
Indexed by manufacturer

Existing mechanisms for messaging:

Write combining → intel p3, p4

Ultrasparc interrupts

Ultrasparc interrupts:

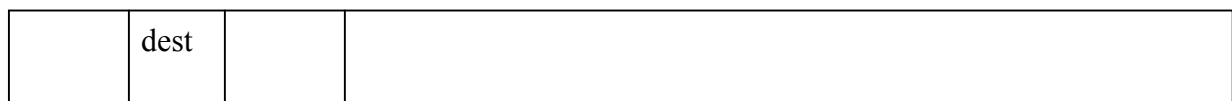


Design uses no interrupt wires. Has 1 interrupt vector.

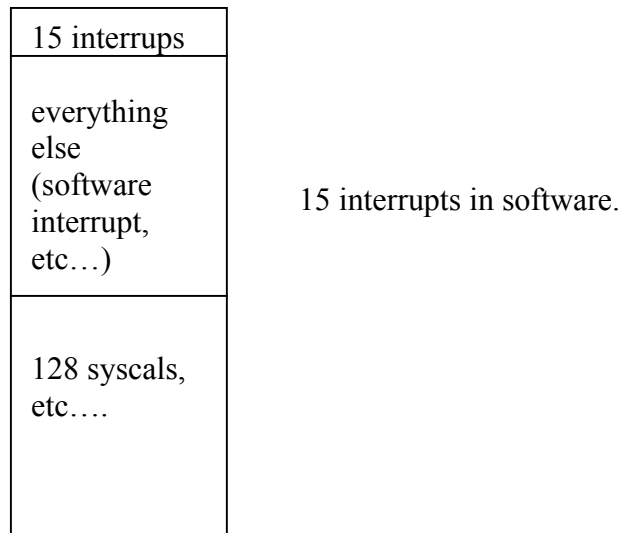
Coprocessor regs are in address space (are NOT L1 cache). Are not user writeable.

Packet on the bus: 32B: 4x8B words: 1<sup>st</sup> is msg hdr. Next 3 are user defined.

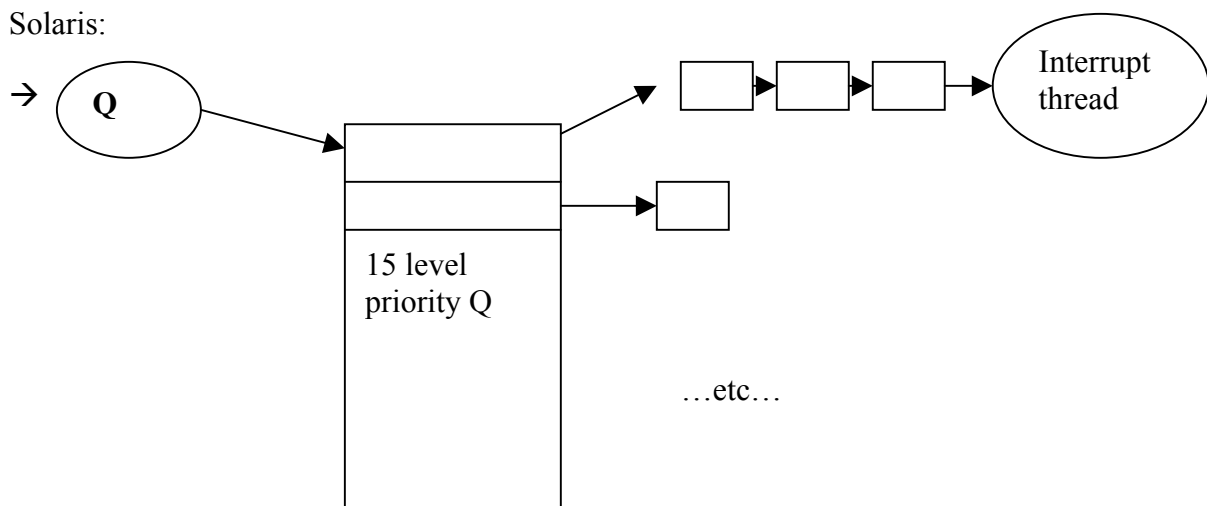
Uses hardware ACK/NACK → Polls status bit. Retry on NACK.



Sun interrupt vector: total of 256 entries



Solaris:



Interrupt thread is like a bottom half in Linux.

Linux:

(Ivan) Similar mechanism in linux.

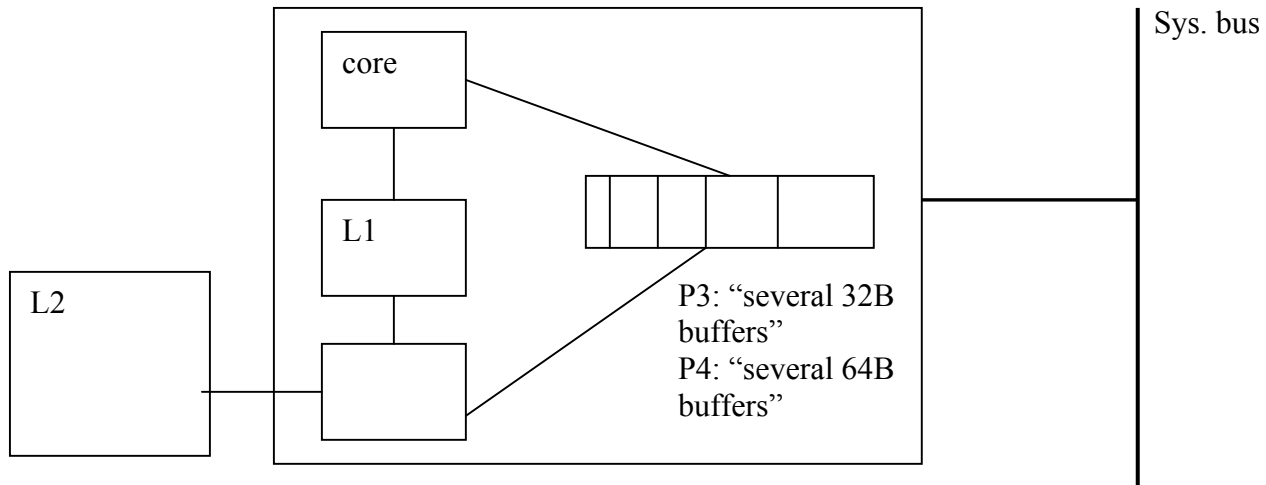
Can forward interrupts on SMP

1. Want to send messages to IO subsystem
  - a. Outgoing: replace sendQ in NI
  - b. Incoming recvQ to notification
2. Protected user level?

- a. Make coprocessor regs unprotected and protect devices
- b. Outgoing: protection check on device #
- c. Incoming: install user code into kernel? Have user level interrupts possibly.

Write combining buffers:

P3/P4



Write combining for uncached messages.

\*need to send cache sized messages.

P3: "several 32B buffers"

P4: "several 64B buffers"

Sys bus has WC empty.

\*this obviously needs to be renamed to WC flush!

Engineers are allowed to have fun too.

1. Decode property of memory

(by page) TLB entries: (WB) WriteBack

(WT) WriteThrough

(UC) Uncached

(SUC) Strong Uncached

(WC) Write Combine

(WPC) ?

WC empty internal unspecified data, fenced operation

2. WC instructions

“non-temporal” store

movnti: move non-temporal int

don't cache, put in WC buffer

allowed to violate traditional memory model

\*assumes you'll write before reading

3. “SWWC” software WC

- Use an L2 cache line as a buffer
- Flush by copy  
w/ld/movnti loop (or MMX/SSE variant)

Conclusion:

How to make either of these a message mechanism?

Let I/O devices write to WC?