

# GEORGIA INSTITUTE OF TECHNOLOGY

College of Computing

## CS6290/CS4290 — High-Performance Computer Architecture Spring 2003

---

CS6290/CS4290 Handout #1  
Introduction and Syllabus

---

Issued: January 6, 2003

- Instructor:** Prof. Ken Mackenzie [kenmac@cc.gatech.edu](mailto:kenmac@cc.gatech.edu)  
Office: CoC 219, x4-1704 WTh4-5.
- Web:** [http://www.cc.gatech.edu/classes/AY2003/cs6290\\_spring/](http://www.cc.gatech.edu/classes/AY2003/cs6290_spring/)
- Lecture:** MWF3-4 in CoC 017 (Fridays are generally discussion)
- Text:** Hennessy and Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufman, 2002 (Third Edition), along with papers to be distributed in class to fuel discussions.
- Description:** This course serves as graduate-level (or advanced undergraduate) introduction to computer architecture. In this course, you will learn about the design and evaluation of computers, particularly advanced (internally parallel) uniprocessors and memory systems.
- Topics:** Memory systems: caching, naming, protection  
Implicitly-parallel architectures: VLIW, superscalar, dataflow  
Out-of-order and speculative execution mechanisms  
Interconnects for parallel processing and for I/O  
Overview of explicitly parallel architectures and emerging hybrids
- Prerequisites:** You should be familiar with computer organization at the level of CS2200. Students cannot receive credit for both CS4290 and CS6290 because the material is the same. Also, ECE6100 is substantially the same course.
- Assignments:** 3 design projects + 6 short homeworks  
1 in-class midterm  
1 final
- Grading:** 15% Homeworks (divided evenly, lowest one dropped)  
45% Projects (15/15/15%)  
15% Midterm Exam  
25% Final  
*CS6290 and CS4290 will be graded independently.*

## Tentative Calendar

<i>(Jan)</i>	<b>6</b> <i>first class</i>	<b>8</b> Review	<b>10</b> VLSI	HW0
	<b>13</b> Review	<b>15</b> Caches	<b>17</b> RISC	HW1
	<b>20</b> <i>holiday</i>	<b>22</b> Caches	<b>24</b> Caches	
<i>(Feb)</i>	<b>27</b> Virtual Memory	<b>29</b> Memory	<b>31</b> VM	HW2
	<b>3</b> Memory	<b>5</b> Review	<b>7</b> Examples	PRJ1
	<b>10</b> <i>midterm</i>	<b>12</b> Pipelines	<b>14</b> ILP	
	<b>17</b> Scheduling	<b>19</b> Scheduling	<b>21</b> Interrupts	HW3
<i>(Mar)</i>	<b>24</b> Interrupts	<b>26</b> Out-of-Order	<b>28</b> SimpleScalar	
	<b>3</b> <i>break</i>	<b>5</b> <i>break</i>	<b>7</b> <i>break</i>	
	<b>10</b> SW pipelines	<b>12</b> Renaming	<b>14</b> Itanium	HW4
	<b>17</b> Prediction	<b>19</b> Predication	<b>21</b> Predictors	PRJ2
	<b>24</b> Power	<b>26</b> Busses	<b>28</b> <i>TBD</i>	
	<b>31</b> Networks	<b>2</b> NIs	<b>4</b> NIs	HW5
<i>(Apr)</i>	<b>7</b> Parallel	<b>9</b> Parallel	<b>11</b> <i>TBD</i>	HW6
	<b>14</b> Examples	<b>16</b> Disks	<b>17</b> <i>TBD</i>	PRJ3
	<b>21</b> <i>TBD</i>	<b>23</b> Review	<b>25</b> <i>TBD</i>	

**Homework and Projects:** Homework consists of relatively short problem sets plus three design projects. The projects consist of paper system designs which are carefully justified using simulation measurements of benchmarks. The simulators and benchmarks are Solaris/SPARC-based and written in C.

**Late Policy:** Homeworks are due at the beginning of the class indicated. Late homework will not be accepted.

**Collaboration:** Unless specifically indicated otherwise, collaboration on projects and homework in **pairs** is welcome and encouraged. If you work in a pair, turn in one write-up with the names of both collaborators. You are welcome to discuss high-level concepts with other groups, but all homework/project solutions must be worked out and written up separately.