

## Extra Notes on the XOR Gate

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The XOR gate shown in class today was slightly trickier than the other CMOS gates. For the normal CMOS gates, if the pulldown (NMOS) network evaluates to true, then the output is false.

A “normal” pulldown network for XOR expresses the following equation:

$$f(X, Y) = X.\bar{Y} + \bar{X}.Y$$

Since this network generates a false/zero/low-voltage output when the expression is true, the gate would implement  $\overline{f(X, Y)}$  (the “XNOR” function). This would need to be followed by an inverter (NOT) to implement an XOR function.

Instead, we could use the following equation for the pull-down network:

$$g(X, Y) = X.Y + \bar{X}.\bar{Y}$$

The overall function (output of the gate would be):

$$\begin{aligned} & \overline{g(X, Y)} \\ &= \overline{X.Y + \bar{X}.\bar{Y}} \\ &= \overline{(X.Y).(\bar{X}.\bar{Y})} \\ &= (\bar{X} + \bar{Y}).(X + Y) \\ &= \bar{X}.X + \bar{X}.Y + \bar{Y}.X + \bar{Y}.Y \\ &= \bar{X}.Y + X.\bar{Y} \end{aligned}$$

Which is the XOR function.