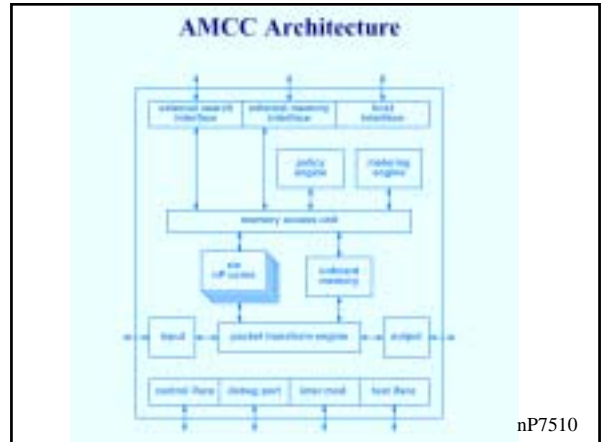


- AMCC fifth generation NPs – nP⁵
- Network optimized Instruction Set Computing
 - RISC + Network Co-processor = “NISC”



Main features

- cluster of nPcores
 - RISC processors augmented with instructions for network processing: byte masking (out of 64b registers), bit manipulations, single instruction CASE statements and other branch instructions...
- many co-processors for networking operations ('engines'); nPcore posts single instruction for functions executed by engines => code size
 - Traffic management (TM)
 - Packet transform engine (PTE)
 - Policy engine (PE)
 - Data coherency/special-purpose unit (SPU)
 - Algorithmic search

Single-stage, single-image processing

- all nPcores execute same program image
- each nPcore:
 - 24 supported tasks/threads
 - 8x8B registers / task
 - instruction pipeline executes 6 instructions, each from different task (i.e. 6 tasks active, zero cycle ctx switch between cycles, hides branch latency etc.)
 - on off-chip access, automatic ctx switch to other ready tasks
- nP3700 – 3 nPcores (target 5Gbps), nP7510 – 6 nPcores (target 10Gbps, solution uses 2 NPUs)
- nPcores share same 64kB program memory, + icache
 - used to have separate program memories each, loaded with same program
- why single-stage, single-image processing?

Traffic Management

- traffic management configurable co-processor
 - hardware support for per-flow queueing/scheduling/admission control for up to 128k flows
 - four-levels of control:
 - 128k flows -> 4k pipes -> 512 subports -> port
 - hardware provides per-flow structures, user uses policy engines to set up traffic -> flow relationship

Exception handling

- AMCC NPs built in support for exception handling by same hardware/software as fast path (flow through)
- ‘exception process flow’ -> for store-and-forward operations
 - exception channel buffer with extra memory
 - e.g., TCP flow termination, assembling jumbo frames

Classification

- On-chip integrated Policy Engine with 512x68bit TCAM with weight-array (and mask arrays)
- large TCAMs expensive ->
- Algorithmic Search Engine – hardware-based mechanism to hash to a memory block in off chip SRAM...

Other engines

- Special Purpose Unit for data coherency
 - ensures atomicity of shared memory accesses – read/modify/write....
- Packet Transform Engine
 - all in/out traffic passes through PTE;
 - does header field prepend/insert/delete, checksums...
 - does not need to wait for entire frame before other processing ‘kicks in’
- Standard interfaces
 - GMII, SPI-3; SPI-4; GPIO; memory controllers...

nPsoft software architecture



AMCC + Control Plane
AMCC + Data Plane
Figure 4. nPsoft Services Framework