



# CS 2200 Fall 2006 Test 2

Name:     Kishore     GT Number: gt                     

1. (1 point, 0 min)

Guess the age of Chris Klaus, the donor of the new COC/ECE building:

(a) ~60      (b) ~25      (c) ~33      (d) ~50

## Pipelined processor

2. (9 points, 10 minutes) (Select one correct choice)

(a) (3 points) (select one correct choice)

With reference to the 5-stage pipelined implementation of LC-2200 instruction set, a second ALU is needed in the EXEC stage of the pipeline

- 1) To make the stage symmetrical
- 2) To enable address calculation for LW/SW instructions
- 3) To enable address calculation for BEQ instruction
- 4) To enable multi-precision arithmetic for ADD instruction
- 5) To enable ADD and NAND instructions to be executed in parallel if they occur one after another

(b) (6 points)

$I_1: R1 \leftarrow R2 + R3$

$I_2: R4 \leftarrow R1 + R5$



If  $I_2$  is immediately following  $I_1$  in the pipeline with no forwarding, how many bubbles will be experienced by the pipeline? **You must explain your answer to get any credit.**

**Three bubbles.**

**The result of the addition by instruction  $I_1$  is written into  $R1$  only at the end of the WB cycle with  $I_2$  waiting in the ID/RR stage for reading  $R1$ .**

# CS 2200 Fall 2006 Test 2

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## Process scheduling

3. (15 points, 10 mins)

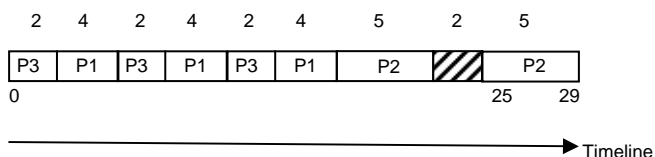
Consider a non-preemptive Shortest Job First (SJF) process scheduler. There are three processes in the scheduling queue and assume that all three of them are ready to run. As the scheduling discipline suggests, always the shortest job that is ready to run is given priority. Scheduling starts at time t=0. The CPU and I/O burst patterns of the three processes are as shown below:

	CPU	I/O	CPU	I/O	CPU	
P1	4	2	4	2	4	<b>P1 is done</b>
P2	5	2	5			<b>P2 is done</b>
P3	2	2	2	2	2	<b>P3 is done</b>

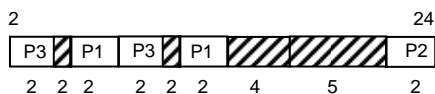
Each process exits the system once its CPU and I/O bursts as shown above are complete.

a) Show the CPU and I/O timelines that result with SJF scheduling from t=0 until all three processes exit the system.

CPU Schedule (SJF)



I/O Schedule



b) What is the waiting time for each process?

**Waiting time:**

**P1 = 2**  
**P2 = 18**  
**P3 = 4**

c) What is the average throughput of the system?

**Total time = 30**

**Throughput = number of processes completed / total time**  
**= 3/30**  
**= 1/10 processes per unit time**

# CS 2200 Fall 2006 Test 2

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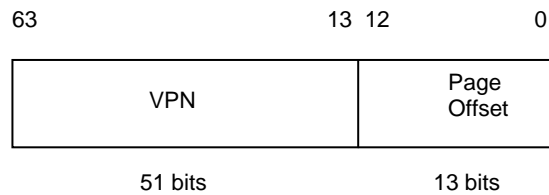
## Virtual Memory and Physical Memory

4. (10 points, 5 mins)

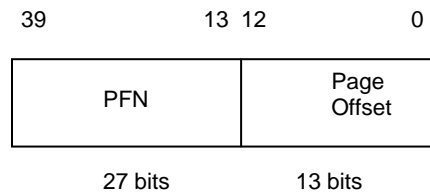
Consider a memory system with 64-bit virtual addresses and 40-bit physical addresses. The page size is 8 KB.

a) Show the layout of the virtual and physical addresses.

Virtual address



Physical address



b) How big is the page table?

**Number of entries in the page table =  $2^{51}$**

c) How many page frames are there in the memory system?

**Number of page frames =  $2^{27}$**

# CS 2200 Fall 2006 Test 2

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## Working Set

5. (10 points, 5 mins)

During the time interval  $t_1 - t_2$ , the following virtual page accesses are recorded for the three processes P1, P2, and P3, respectively.

P1: 0, 10, 1, 0, 1, 2, 10, 2, 1, 1, 0

P2: 0, 100, 101, 102, 103, 0, 101, 102, 104

P3: 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5

a) What is the **working set** for each of the above three processes for this time interval?

P1's Working set = {0, 1, 2, 10}

P2's Working set = {0, 100, 101, 102, 103, 104}

P3's Working set = {0, 1, 2, 3, 4, 5}

b) What is the **cumulative memory pressure** on the system during this interval?

Cumulative memory pressure = sum of the working sets of all processes  
= 4 + 6 + 6  
= 16 page frames

## Page replacement

6. (10 points, 10 mins)

Given the before picture of the page manager's data structure as shown below, show the contents of the data structures after P1's page fault at VPN = 2 is serviced. The victim page frame chosen by the page replacement algorithm is PFN = 84. Note that only relevant entries of the Frame Table are shown in the Figures.

# CS 2200 Fall 2006 Test 2

Name:     Kishore     GT Number: gt                     

BEFORE THE PAGE FAULT

	PFN	V
VPN = 0	50	V
VPN = 1	52	V
VPN = 2	--	I
VPN = 3	60	V

P1's PT

	PFN	V
VPN = 0	70	V
VPN = 1	80	V
VPN = 2	85	V
VPN = 3	84	V

P2's PT

0	....
	....
50	<P1, 0>
52	<P1, 1>
60	<P1, 3>
70	<P2, 0>
80	<P2, 1>
84	<P2, 3>
85	<P2, 2>

Frame Table

AFTER THE PAGE FAULT FOR P1 at VPN = 2 (FILL IN THE DATA STRUCTURES WITH YOUR ANSWER)

	PFN	V
VPN = 0	50	V
VPN = 1	52	V
VPN = 2	84	V
VPN = 3	60	V

P1's PT

	PFN	V
VPN = 0	70	V
VPN = 1	80	V
VPN = 2	85	V
VPN = 3	--	I

P2's PT

0	....
	....
50	<P1, 0>
52	<P1, 1>
60	<P1, 3>
70	<P2, 0>
80	<P2, 1>
84	<P1, 2>
85	<P2, 2>

Frame Table

# CS 2200 Fall 2006 Test 2

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## Effective Memory Access Time (EMAT)

7. (10 points, 10 min)

Consider the following memory hierarchy:

- L1 cache: Access time = 2ns; hit rate = 99%
- L2 cache: Access time = 5ns; hit rate = 95%
- L3 cache: Access time = 10ns; hit rate = 80%
- Main memory: Access time = 100ns

Compute the effective memory access time.

$$\text{EMAT}_{L3} = L3\text{'s hit rate} * L3\text{'s access time} + \\ L3\text{'s miss rate} * \text{Main memory access time}$$

$$\text{EMAT}_{L3} = 0.8 * 10 + 0.2 * 100 \\ = 28$$

$$\text{EMAT}_{L2} = L2\text{'s hit rate} * L2\text{'s access time} + L2\text{'s miss rate} * \text{EMAT}_{L3}$$

$$\text{EMAT}_{L2} = 0.95 * 5 + 0.05 * 28 \\ = 4.75 + 1.4 \\ = 6.15$$

$$\text{EMAT} = L1\text{'s hit rate} * L1\text{'s access time} + L1\text{'s miss rate} * \text{EMAT}_{L2}$$

$$\text{EMAT} = 0.99 * 2 + 0.01 * 6.15 \\ = 1.98 + .0615 \\ = 2.0415 \text{ ns}$$

# CS 2200 Fall 2006 Test 2

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## Effect of Memory Hierarchy on Pipeline Performance

8. (15 points, 10 mins)

Consider a pipelined processor:

- Average CPI without accounting for memory stalls = 1.5.
- I-Cache hit rate = 95%.
- D-Cache hit rate = 98%.
- Assume that memory reference instructions account for 20% of all the instructions executed. Out of these 80% are loads and 20% are stores.
- Read-miss penalty = 20 cycles.
- Write-miss penalty = 5 cycles.

Compute the effective CPI of the processor accounting for the memory stalls.

$$\begin{aligned}\text{Effect of I-cache on CPI} &= \text{I-cache miss rate} * \text{read-miss penalty} \\ &= 0.05 * 20 = 1 \text{ cycle}\end{aligned}$$

$$\begin{aligned}\text{Effect of loads} &= (\% \text{ loads}) * \text{D-cache miss rate} * \text{read-miss penalty} \\ &= 0.8 * 0.02 * 20 = 0.32\end{aligned}$$

$$\begin{aligned}\text{Effect of stores} &= (\% \text{ stores}) * \text{D-cache miss rate} * \text{write-miss penalty} \\ &= 0.2 * 0.02 * 5 = 0.02\end{aligned}$$

$$\begin{aligned}\text{Effect of D-cache on CPI} &= (\% \text{ memory ref instructions}) \\ &\quad * (\text{Effect of loads} + \text{Effect of stores}) \\ &= 0.2 * (0.32 + 0.02) \\ &= 0.068\end{aligned}$$

$$\begin{aligned}\text{Effective CPI} &= \text{base CPI} + \text{Effect of I-cache on CPI} \\ &\quad + \text{Effect of D-cache on CPI} \\ &= 1.5 + 1 + 0.068 \\ &= 2.568\end{aligned}$$

# CS 2200 Fall 2006 Test 2

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## Cache design

9. (20 points, 20 mins)

Consider a 4-way set-associative cache.

- Total data size of cache = 256KB.
- CPU generates 32-bit byte-addressable memory addresses.
- Each memory word consists of 4 bytes.
- The cache block size is 32 bytes.
- The cache has one valid bit per cache line.
- The cache uses write-back policy with one dirty bit per word.

a) Show how the CPU interprets the memory address (i.e., which bits are used as the cache index, which bits are used as the tag, and which bits are used as the offset into the block?).

Tag            16 bits (31 to 16)  
Index         11 bits (15 to 5)  
Block offset  5 bits ( 0 to 4)

b) Compute the total size of the cache (including data and metadata). You have to show partial work to get any credit.

Four 4 parallel caches each with 2K blocks.

For each cache:

Tag = 16 \* 2048 bits

Valid = 2048 bits

Dirty = 8 \* 2048 bits

Total metadata = 25 \* 2048 (sum of the above)

Metadata for entire 4-way set associative cache

= 4 \* 25 \* 2048 bits

= 25 Kbytes

Total cache size

= data + metadata

= 256 KB + 25 KB

= 281 Kbytes