

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

Network protocols

2. (15 points, 20 mins)

You are given the following:

Message size	=	1900 Kbits
Header size per packet	=	1000 bits
Packet size	=	20 Kbits
Bandwidth on the wire	=	400,000 bits/sec
Time of flight	=	2 secs
Window size	=	10
Sender overhead	=	0
Receiver overhead	=	0
Size of ACK message	=	negligible (take it as 0)

(a) (5 points) Assuming a 10% packet errors on DATA packets (no errors on ACK packets, and no lost packets), how many total DATA packets are transmitted by the sender to accomplish the above message delivery?

(b) (10 points) Assuming an error free network, compute the total time to accomplish the above message delivery. You must show your work (such as timing diagram) to get partial credit.

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

File system (i-nodes)

3. (15 points, 20 mins)

- (a) (10 points) Given the following commands pictorially show the i-nodes and their contents. You can fabricate disk block addresses for the i-nodes to make the pictures simpler. Where relevant show the reference count for the i-nodes.

```
touch /tmp/foo
mkdir /tmp/bar
mkdir /tmp/bar/gag
ln /tmp/foo /tmp/bar/foo2
ln -s /tmp/foo /tmp/bar/foo
ln /tmp/foo /tmp/bar/gag/foo
ln -s /tmp/bar /tmp/bar/gag/bar
ln -s /tmp /tmp/bar/gag/tmp
```

Note:

mkdir creates a directory; touch creates a zero byte file; ln is link command (-s denotes symbolic link).

Assume that the above files and directories are the only ones in the file system.

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

(b) (5 points) If we now execute the command:

```
rm /tmp/bar/foo
```

Show the new contents of the i-nodes. (SHOW ONLY THE AFFECTED I-NODES).

File system (user level)

4. (5 points, 5 mins)

Given the following:

Number of cylinders on the disk	=	10,000
Number of platters	=	10
Number of surfaces per platter	=	2
Number of sectors per track	=	128
Number of bytes per sector	=	256
Disk allocation policy	=	contiguous cylinders

(a) How many cylinders should be allocated to store a file of size 3 Mbyte?

(b) How much is the internal fragmentation caused by this allocation?

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

Disk scheduling

5. (9 points, 10 mins)

Given the following:

Total number of cylinders in the disk	=	200
Current head position	=	cylinder 23
Current requests in order of arrival	=	20, 17, 55, 35, 25, 78, 99

(a) Show the schedule for C-LOOK for the above requests

(b) Show the schedule for SSTF

(c) Show the schedule for LOOK

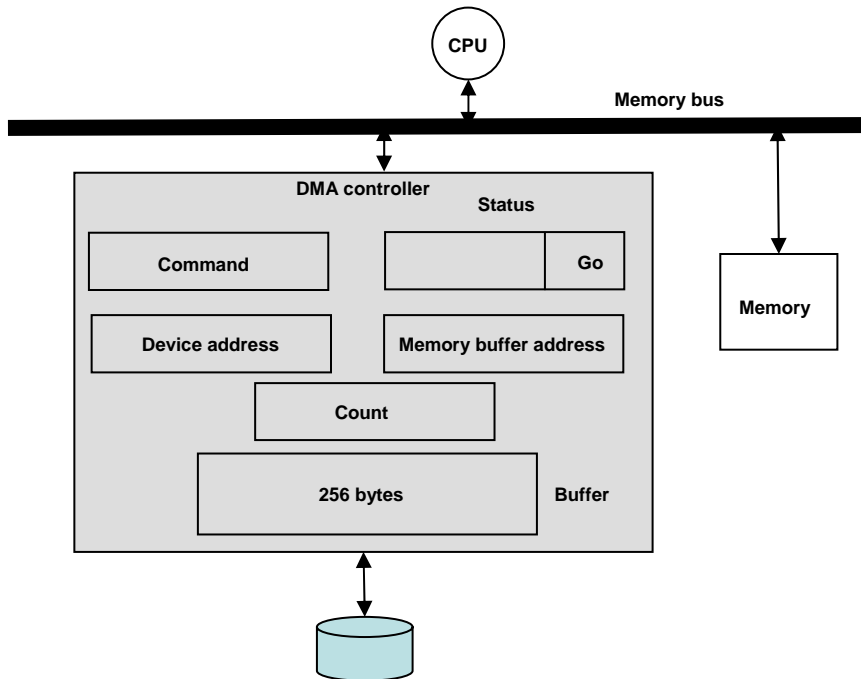
CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

I/O

6. (5 points, 10 mins)

Given the following device controller:



Write the sequence of instructions (pseudo instructions will suffice, need not be actual assembly instructions) that the CPU has to execute to move N bytes of data starting from device address D to memory address starting at M .

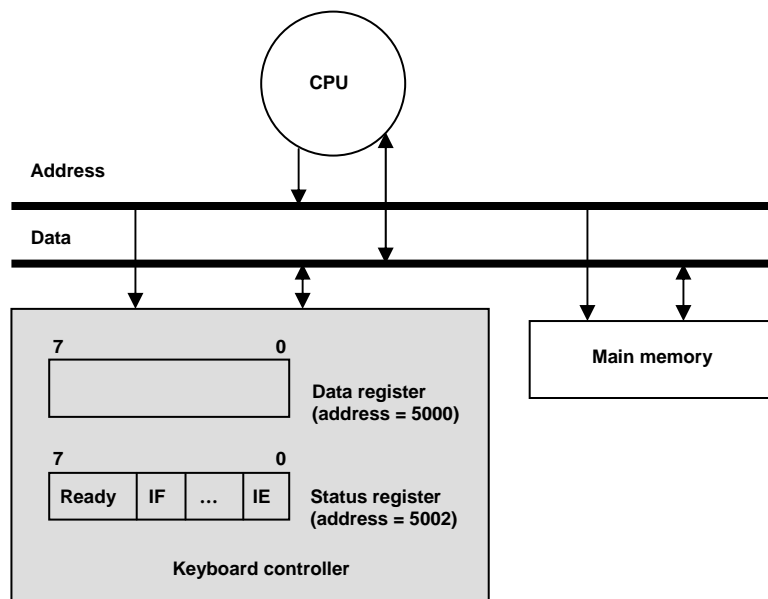
CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

I/O

7. (5 points, 10 mins)

Give the following device controller:



Write the sequence of instructions (pseudo instructions will suffice, need not be actual assembly instructions) that the CPU has to execute to read a character from the device and store to some memory location M.

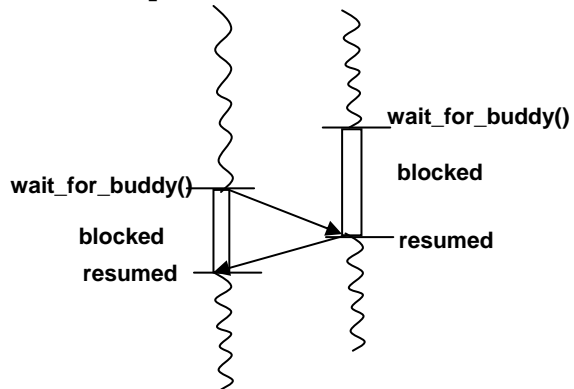
CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

Threads Rendezvous

8. (10 points, 20 mins)

The function `wait_for_buddy()` is used by EXACTLY 2 threads to rendezvous with each other as shown in the figure below. The order of arrival of the two thread should be immaterial. At the indicate places in the function, insert code that will accomplish the intended rendezvous.



```
boolean buddy_waiting = FALSE;
mutex_lock mtx; /* assume this has been initialized properly */
cond_var cond; /* assume this has been initialized properly */

wait_for_buddy()
{
    lock(mtx);

    if (buddy_waiting == FALSE) {
        /****** need some code here *****/

        wait (cond, mtx);

        /****** need some code here *****/
    }
    else {
        /****** need some code here *****/

        signal (cond);

        /****** need some code here *****/
    }

    /****** need some code here *****/
}
```

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

Multiprocessor Cache Coherence

9. (10 points, 10 mins)

Given the following details about an SMP (symmetric multiprocessor):

Cache coherence protocol: **write-invalidate**

Cache to memory policy: **write-back**

Initially:

The caches are empty

Memory locations:

A contains 10

B contains 5

Consider the following timeline of memory accesses from processors P1, P2, and P3.

Time (in increasing order)	Processor P1	Processor P2	Processor P3
T1	Load A		
T2		Load A	
T3			Load A
T4		Store #40, A	
T5	Store #30, B		

Fill the table below. We have started it off for you at time T1.

(**I** indicates the cache location is invalid. **NP** indicates not present)

Time	Variables	Cache of P1	Cache of P2	Cache of P3	Memory
T1	A	10	NP	NP	10
T2	A				
T3	A				
T4	A				
T5	A				
	B				

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

Virtual Memory

10. (5 points, 5 mins)

Given the following:

Virtual address 40 bits

39

0

Physical address 24 bits

23

0

Page size 8 K Bytes

A direct mapped TLB with 256 entries

Answer the following:

(a) The number of tag bits per TLB entry is _____
(show your work here)

(b) The number of bits per TLB entry to store page frame address is _____
(show your work here)

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

Memory hierarchy

11. (10 points, 15 mins)

Given the following:

Total number of blocks in a 2-way set associative cache: 8

Assume LRU replacement policy

	C1	C2
0		
1		
2		
3		

Given the following memory accesses shown in the table below, indicate the cache which will host the memory location and the specific cache index where it will be hosted, and in case of a miss the type of miss (cold/compulsory, capacity, conflict). To help you along we have filled out the first couple of memory accesses.

Memory location	C1	C2	Hit/miss	Type of miss
0	Index = 0		Miss	Cold/compulsory
16		Index = 0	Miss	Cold/compulsory
1	Index = 1		Miss	Cold/compulsory
2				
0				
8				
0				
8				
16				
0				
1				
2				
3				
4				
5				
6				
7				
16				

CS 2200 Spring 2006 Final Section B

Name: _____ GT Number: gt _____

Pipelining

12. (10 points, 10 mins)

(a) (5 points)

I₁: R1 ← R2 + R3

I₂: R4 ← R1 + R5



If I₂ is immediately following I₁ in the pipeline with no forwarding it will results in

- _____ Zero bubbles
- _____ One bubble
- _____ Two bubble
- _____ Three bubbles
- _____ Four bubbles

(b) (5 points)

Branch target buffer is

- _____ An area of memory reserved for branch instructions
- _____ A hardware device that keeps the outcome and target addresses of recent branches encountered during the program execution
- _____ A hardware device that is pre-loaded before the program starts with the expected outcome and the target addresses of the branches in the program
- _____ An extra stage in the pipeline for efficient handling of control hazards