

Homework 1

Prof. Loh

CS6290 - Spring 2007

Handed Out: 22 Jan 2007 (Mon)

Due: 31 Jan 2007 (Wed)

1. Yield

- (a) H&P, problem 1.1, parts (a) and (b)

2. Performance

- (a) H&P, problem 1.12, parts (a)-(f)
 (b) H&P, problem 1.14, parts (a) and (b)

3. ILP Consider the following code:

```

top: (A)  DIV.D      F0,F2,F4      ; F0 is dest, F2, F4 are sources
      (B)  ADD.D      F6,F0,F8
      (C)  S.D        F6,0(R1)    ; note: F6 is a source
      (D)  SUB.D      F8,F10,F12
      (E)  MUL.D      F6,F10,F8
      (F)  DADDUI     R1, R1, #4   ; #4 is a constant
      (G)  DSUBUI     R2, R2, #1
      (H)  BEQZ       R2, top     ; note: R2 is a source
  
```

- (a) List all WAR dependencies within a single iteration
 (b) List all WAW dependencies within a single iteration
 (c) List all RAW dependencies within and between two iterations
 (d) Draw two (or more) iterations of the dataflow graph when RAW, WAR, WAW and control dependencies are all enforced. What is the ILP for n iterations of this graph? What is the ILP for $\lim_{n \rightarrow \infty}$?
 (e) Repeat, but only when true RAW dependencies are enforced.

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4. Compiler Support for ILP

- (a) H&P, problem 2.1
- (b) H&P, problem 2.2
- (c) H&P, problem 2.3
- (d) H&P, problem 2.5

5. HW Register Renaming

- (a) H&P, problem 2.7