

CS8803HPC : High Performance Communications

Spring 2008 Syllabus

Meeting Times: Mon/Wed, 3:05-4:25PM, Cherry Emerson 322

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Office Hours: TDB

Web page: http://www.cc.gatech.edu/classes/AY2008/cs8803hpc_spring/

Course Outline:

This project-based course covers issues in high-performance communication, ranging from architecture and devices, to interconnection networks, network interfaces and network processors, protocols and standards, OS and middleware support, as well as driving applications from the scientific and enterprise domain, and evaluation and development tools. The course contains a significant laboratory component which may be based on platforms such as Intel's IXP2xxx network processors, Infiniband-based platforms, modern multi-core machines, or may target other specialized accelerators. Alternative equipment bases are permissible, subject to instructor approval. The coursework is based on a series of research papers, industry white papers on novel products, software tools and technologies, and chapters from select titles. The course is intended for graduate or advanced undergraduate students with background in architecture (CS4290/CS6290), networking (CS4251) or operating systems (CS4210/CS6210).

Textbooks:

No textbook is required for the course.

Exams:

No exams.

Project:

The focus of the course project is to develop, analyze and experiment with technologies which address communications-related bottlenecks in various application domains on modern platforms. Select topics of interest include application/protocol/kernel stack splitting for multi-core platforms; communication acceleration solutions via offload to programmable network interconnection hardware (e.g., IXP network processors) or other specialized accelerators (Cell, GPUs, FPGAs) and/or OS- or application-bypass techniques (e.g., TCP on IXP, FTP over IB); solutions which address impedance mismatches in local-/cluster- vs. wide-area settings; high-performance communication services which address applications' reliability, security, resource reservation/isolation (i.e., virtualization) requirements; high performance protocols (e.g., RDMA, SCTP) and communication architectures (e.g., OpenIB/Open Fabric, Portals); benchmark or simulation module development,

etc. Permissible development platforms include Intel's IXP 2xxx network processors, Infiniband architecture, kernel-level development on multi-core or embedded platforms, or alternate hardware (e.g., graphics cards, FPGAs) subject to instructor approval.

Grading:

60% project: 40% - implementation, 10% - report, 10% - presentation;
15% - paper presentation;
15% - two homework assignments;
10% - class participation

Homework and Assignment Due Times:

Homeworks are due by class time on the due date (either by email before class or as hardcopy in class). Complete project turn-in is due by last class of the semester.

Late Penalty Policy (only for homework assignments):

This late penalty policy is 5% penalty for each day late, up to 5 days (25%).

Honor Code:

The Institute Student Conduct Code is printed on pages 336-339 of the GT General Catalog. You and I are expected to abide by it. I do not deal with cases of academic misconduct in person (the Office of the Senior Associate Dean of Students will be notified).