Selector
Image of a selector:

Reference: http://www.edwardbosworth.com/My5155Text_V07_HTM/MyText5155_Ch06_V07.htm

Barrel shifter
Image of 4 bit barrel shifter where C = 1:

Reference: http://www.edwardbosworth.com/My5155Text_V07_HTM/MyText5155_Ch06_V07.htm

4 bit barrel shifter has 4x inputs and 2s inputs (s inputs to specify how many bits to shift)

Example of a right cyclic shift: 101011 -> 110101

Barrel shifter is hardware logic to implement cyclic shift
Used also in computer architecture

Priority Scheduler
- First 1 in inputs from left is the only 1 value outputted
- Input: 0011 -> Output: 0010
- Useful for requests and only letting one input to access resource at a time
- If all inputs are 0 all outputs are 0

\[ o_1 = i_1 \]
\[ o_2 = i_1 \cdot i_2 \]
... 
\[ o_k = i_1 \cdot i_2 \cdot \ldots \cdot i_{k-1} \cdot i_k \]

Area is important because of chip size. Goal is to optimize area and delay and to find the optimum tradeoff between the two.

Given these inputs n is a power of 2
- \{i_1 \cdot i_2\}, \{i_3 \cdot i_4\}, \{i_5 \cdot i_6\}, \{i_7 \cdot i_8\} 2 in a block, need n/2 gates
- \{i_1 \cdot i_2 \cdot i_3 \cdot i_4\}, \{i_5 \cdot i_6 \cdot i_7 \cdot i_8\} 4 in a block, need n/4 gates
... 
Area: \(O(n)\), Delay: \(\log(n)\)

At most \(n\) \begin{align*}
o_{12} &= i_1 \cdot i_2 \cdot i_3 \cdot \ldots \cdot i_{11} \cdot i_{12} \\
&= 11 = (1011)_{2} \\
&= (i_1, i_2, \ldots, i_{8}) \cdot (i_9, i_{10}) \cdot (i_{11})
\end{align*}

Area: \(n \cdot \log(\log(n))\)
Delay: \(\log(n) + \log(\log(n)) = \log(n \cdot \log(n))\)