

# GEORGIA INSTITUTE OF TECHNOLOGY

College of Computing

## CS/EE6760 — Parallel Computer Architecture I

Fall 1998

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CS/EE6760 Handout #2  
Papers

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Issued: September 24, 1998

This is the tentative reading list. Papers will be distributed in class.

### General

1. [Wood95] D. A. Wood and M. D. Hill, “Cost-Effective Parallel Computing”, *IEEE Computer*, 28(2), pages 69-72, February, 1995.
2. [Patterson85] David A. Patterson, “Reduced Instruction Set Computers”, *Communications of the ACM*, 28(1), pages 8-21, January, 1985.

### Memory Systems

3. [Dennis65] Jack B. Dennis, “Segmentation and the Design of Multiprogrammed Computer Systems”, *Journal of the Association for Computing Machinery*, 12(4), pages 589-602, October, 1965.
4. [Jouppi90] N. P. Jouppi, “Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers” in *Proceedings of the 17th Annual International Symposium on Computer Architecture (ISCA)*, pages 364-373, June, 1990.
5. [Wang89] W. Wang, J. Baer and H. M. Levy, “Organization and Performance of a Two-Level Virtual-Real Cache Hierarchy” in *Proceedings of the 16th Annual International Symposium on Computer Architecture (ISCA)*, pages 140-148, June, 1989.
6. [Song97a] Peter Song, “Direct RDRAM Sustains 1.5 Gbytes/s”, *Microprocessor Report*, 11(14), October 27, 1997.

## Instruction-Level Parallelism

7. [Fisher91] Joseph A. Fisher and B. Ramakrishna Rau, “Instruction-Level Parallel Processing”, *Science*, 253, pages 1233-1241, September 13, 1991.
8. [Smith88] J. E. Smith and A. R. Pleszkun, “Implementing Precise Interrupts in Pipelined Processors”, *IEEE Transactions on Computers*, 37(5), pages 562-573, May, 1988.
9. [Palacharia97] Subbarao Palacharia, Norman P. Jouppi and J. E. Smith, “Complexity-Effective Superscalar Processors” in *Proceedings of the 24th Annual International Symposium on Computer Architecture*, pages 206- 218, June, 1997.
10. [Colwell88] Robert P. Colwell, Robert P. Nix, John J. O’Donnell, David B. Papworth, and Paul K. Rodman, “A VLIW Architecture for a Trace Scheduling Compiler”, *IEEE Transactions on Computers*, 37(8), pages 967-979, August, 1988.
11. [Gwennap96] Linley Gwennap, “Digital 21264 Sets New Standard”, *Microprocessor Report*, 10(14), October 28, 1996.
12. [Song97] Peter Song, “UltraSparc-3 Aims at MP Servers”, *Microprocessor Report*, 11(14), October 27, 1997.
13. [Gwennap97] Linley Gwennap, “Intel, HP Make EPIC Disclosure”, *Microprocessor Report*, 11(14), October 27, 1997.
14. [August98] David I. August, Daniel A. Connors, Scott A. Mahlke, John W. Sias, Kevin M. Crozier, Ben-Chung Cheng, Patrick R. Eaton, Qudus B. Olaniran and Wen-mei W. Hwu, “Integrated Predicated and Speculative Execution in the IMPACT EPIC Architecture” in *Proceedings of the 25th Annual International Symposium on Computer Architecture (ICSA)*, June, 1998.

## Multiprocessors

15. [Dally91] William J. Dally, D. Scott Wills and Richard Lethin, “Mechanisms for Parallel Computers” in *Proceedings of the NATO Advanced Study Institute on Parallel Computing on Distributed Memory Multiprocessors*, Springer-Verlag, 1991.
  16. [vonEicken92] Thorsten von Eicken, David E. Culler, Seth Copen Goldstein and Klaus Erik Schauser, “Active Messages: a Mechanism for Integrated Communication and Computation” in *Proceedings of the 19th Annual International Symposium on Computer Architecture (ISCA)*, May, 1992.
  17. [Kubiatowicz93] John Kubiatowicz and Anant Agarwal, “Anatomy of a Message in the Alewife Multiprocessor” in *Proceedings of the 7th ACM International Conference on Supercomputing (ICS)*, July, 1993.
  18. [Laudon97] James Laudon and Daniel Lenoski, “The SGI Origin: A ccNUMA Highly Scalable Server” in *Proceedings of the 24th Annual International Symposium on Computer Architecture (ISCA)*, June, 1997.
  19. [Scott96] Steven L. Scott, “Synchronization and Communication in the T3E Multiprocessor” in *Proceedings of the Seventh International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 26-36, October, 1996.
- one or two others TBD

## Blue Sky

20. [Ebcioglu97] Kemal Ebcioglu and Erik R. Altman, “DAISY: Dynamic Compilation for 100% Architectural Compatibility” in *Proceedings of the 24th Annual International Symposium on Computer Architecture (ISCA)*, pages 26-37, June, 1997.
21. [Sohi95] Gurindar S. Sohi, Scott E. Breach, and T. N. Vijaykumar, “Multiscalar Processors” in *Proceedings of the 22nd Annual International Symposium on Computer Architecture (ISCA)*, pages 414-425, June 1995.