GEORGIA INSTITUTE OF TECHNOLOGY

College of Computing

CS/EE6760 — Parallel Computer Architecture I

Fall 1998

CS/EE6760 Handout #1 — Issued: September 24, 1998

Introduction and Syllabus

Instructor: Ken Mackenzie — kenmac@cc.gatech.edu

Office: CCB 219, x4-1704 — WTh3-5 or by appt.

Assistant: Jalisa Norton, CCB 264, x4-9760

TA: Li Zou — zou@cc.gatech.edu

Office: (common area) — hours TTh10-11

Web: http://www.cc.gatech.edu/~kenmac/6760/

Lecture: TTh1:30-3:00 in Weber SS&T, room 1

Text: Hennessy and Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufman, 1995 (Second Edition), along with a number of papers to be distributed in class.

Prerequisites: You should be familiar with computer organization at the level of CS3760. CS students cannot receive credit for both CS6760 and CS4760.

Description: This course serves as a graduate-level introduction to computer architecture. In this course, you will learn about the design and evaluation of advanced (internally parallel) uniprocessors, memory systems and explicitly parallel computer architectures.

Topics: Memory systems: naming, protection, caching.
Instruction-level parallelism:
    pipelined, out-of-order and speculative architectures.
Interconnects (for parallel processing or for I/O)
Explicitly parallel architectures:
    communication/synchronization models and mechanisms,
Emerging hybrid architectures.

Assignments: 4 homeworks
3 short design projects
1 in-class midterm, 1 final

Grading: 20% Homeworks (5% each)
30% Projects (5/10/15%)
50% Exams (20% midterm plus 30% final)

Tentative Calendar

(Sep)			**24**	Introduction	
	29	Memory *(hw0 due)*	**1**	Memory	
(Oct)	**6**	*(no class)*	**8**	Memory	*(hw1 due)*
	13	ILP	**15**	ILP	*(prj1 due)*
	20	ILP	**22**	ILP	*(hw2 due)*
	27	ILP	**29**	Review	*(prj2 due)*
(Nov)	**3**	Midterm	**5**	Interconnects	
	10	Multiprocessors	**12**	Multiprocessors	*(hw3 due)*
	17	Multiprocessors	**19**	Multiprocessors	*(hw4 due)*
	24	Multiprocessors	**26**	*(no class)*	
(Dec)	**1**	*(prj3 due)*	**3**	Review	

Projects

Some of the homework consists of short projects. These are small design projects where the designs are to be justified using measurements from simulations of benchmarks. The challenge, then, is both coming up with designs as well as developing appropriate simulation experiments. The simulators and benchmarks are Sparc-based.

Collaboration:

Unless specifically indicated otherwise, collaboration on projects and homework in **pairs** is encouraged. Note that pairs consisting of one person from ECE and one from CS are particularly likely to be useful. If you work in a pair, turn in one write-up with the names of both collaborators. You're welcome to discuss high-level concepts with other groups, but all homework solutions must be worked out and written up separately.

Late Policy:

Homeworks are due at the beginning of the class indicated. Late homework will not be accepted.