Kaushik Ghosh

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Objective

To acquire a position which requires strengths in one or more items of my areas of interest, as mentioned below.

Areas of Interest

- Computer operating systems, especially, parallel and distributed operating systems. Scalable system support for large servers. Schedulers and synchronization protocols.
- High-Performance computer networks.
- Real-time computer systems. Operating systems support for multimedia.
- Parallel discrete-event simulation, including real-time simulation.
- Performance analysis of computer systems through simulation and experimental evaluation.
- Software design and development.

Education

Ph.D. in Computer Science, September 1995.
Georgia Institute of Technology, Atlanta, GA.
Dissertation Title: *Speculative Execution in Real-Time Systems.*
Advisors: Prof. Richard M. Fujimoto and Prof. Karsten Schwan.

M.S. in Computer Science, December 1991.
Georgia Institute of Technology, Atlanta, GA.
Grade Point Average: 3.9/4.0

B.Tech. in Computer Science and Engineering, May 1989.
Indian Institute of Technology, Kharagpur, India.
Grade Point Average: 9.3/10.0
Dissertation topics: Expert System building tools, and efficient 2-dimensional representation of 3-dimensional spatial information using voxels.

Computer Systems and Languages

- Fluent in C, C++, Fortran, Pascal.
- Experience with Unix, and PThreads; working knowledge of Mach. Experience with message-passing libraries, including PVM and MPI.
- Experience with parallel programming and parallel machines, including the Kendall Square Research machine, SGI Challenge, PowerChallenge and Origin-2000, BBN Butterfly, Sequent Symmetry, and with SGI and Sun workstations.

Experience

- 07/95 - present: Full-time employee with the Operating Systems and Network Software groups at Silicon Graphics Inc., Mountain View.
  - Developing systems software for high-performance operating systems and tools.
  - Pursuing reflective memory technology for low-latency message-passing on a cluster of Challenge and/or Power Challenge machines. Modifying reflective memory drivers to work on a 64-bit operating system. Use of safe user-level DMA for high performance from such memory systems.
  - mpirun – a front-end to SGI's MPI library. Apart from being a parser, it performs job-launching, as well as primitive load-balancing on the various hosts known to the cluster.
  - Firmware and protocol development for high-performance message-passing between Challenge and/or Power Challenge machines over HIPPI, by bypassing the operating system – essentially creating a minimal custom protocol stack for symmetric multiprocessors. Message bandwidth (between hosts) seen by the application is within 3% of theoretical hardware (HIPPI) bandwidth; message latency between hosts as seen by the application is under 100 microseconds. Being used by MPI, and databases.
  - Primitives for fast but safe communication between applications running on distinct partitions of Origin-2000 – SGI's new distributed memory multiprocessor machine (each partition runs a distinct copy of the OS). This is performed by opening up the firewall between partitions for certain "well-known" regions, mapping such regions into user-space, and using the underlying hardware-cache-coherence mechanism – utilizing SGI's custom high-performance interconnect (Craylink) – to advantage. This affords extremely low-latency *and* high bandwidth communication between user applications running on the distinct partitions. To be used by MPI.
  - A software library for guaranteeing certain rates of input/output to/from devices connected to SGI's new non-uniform-memory-access machines. In order to do this, the drivers for the devices in question were modified to support certain additional entry-points specific to reserving/allocating bandwidths. Further, all the components – buses, bridges, memory controllers, etc. – in the path from device to memory were modeled (and bandwidth reservation on these components implemented) to ensure that extraneous applications cannot prevent an application that is actually using the library from getting its guaranteed bandwidth. Finally, new functionality was added to the operating system kernel to discover the path from the source to the sink of a guaranteed bandwidth stream, to consider disparate devices through a uniform software interface, and to handle memory-migration issues. To be used by video-on-demand and other real-time applications.
  - Network protocol design and development for *Scheduled Transfers* (ST) – a new ANSI standard. Includes not only the networking aspects in the kernel and user-level, but also integration with other parts of the kernel/filesystem, so that SGI's Bulk Data Server (BDS) can make efficient use of ST over HIPPI-800 and HIPPI-6400. This is work-in-progress.
  - General familiarization and bug-fixes on different versions of the IRIX kernel, and MPI.
- 06/94 - 09/94: Summer Intern at Sun Microsystems Inc., Mountain View.
  - On-line monitoring of distributed programs, and display of the monitored information. This work was done on Spring – Sun's new Distributed Operating System. Implemented tabulators, controllers, and matrix-viewers, which are tools that afford a graphical and controllable interface to any object in the system. Object attributes are not only visible, but also dynamically modifiable from the controllable interface. Integrated Mosaic into Spring's tabulators and controllers. Extensive use of IDL for interface definition in all these tools.

- 06/93 - 09/93: Summer Intern at Kendall Square Research, Massachusetts.
  - Designed and implemented protocols for fast message passing via the shared memory on KSR computers. Ported and tuned two widely used message passing libraries – TCGMSG (from Argonne National Laboratories) and PVM (from Oak Ridge National Laboratories) – for the KSR multiprocessor. Obtained message transfer rates of about 11 MBytes/sec on TCGMSG and 10 MByte/sec on PVM.
- 09/90 - 6/95: Research Assistant at the College of Computing, Georgia Tech. Projects related to Parallel Operating Systems, Parallel Programming Environments, Parallel Discrete-Event Simulation, and Real-Time Systems.
  - Implemented a user-level threads package (with the same interface as Mach CThreads) on the Kendall Square Research multiprocessor. The system software on this multiprocessor comes equipped with PThreads, which are kernel-level threads. The CThreads layer implemented performs an order of magnitude faster than PThreads (for certain functions like thread forking, and locking). Using the package to monitor application programs.
  - Designed and implemented a shared-memory abstraction called Space-Time Memory. It allows processors executing events with different timestamps in a parallel discrete-event simulation to have a coherent view of memory (memory is versioned for this purpose). Programmed two applications – a benchmark called the Sharks World, and a combat simulation – to demonstrate the efficacy of the abstraction and implementation. (Implemented on the Butterfly and the KSR multiprocessors.)
  - Added a layer over the event-oriented Time-Warp simulation testbed available at the College of Computing at Georgia Tech to provide a powerful process-oriented interface to the Time-Warp kernel for different simulation languages (e.g., SIMSCRIPT, ModSim, and eventually C), for automatic optimistic parallelization of applications written in these languages. (Implemented on the Butterfly and the KSR multiprocessors.)
  - Examining the effects of using Time-Warp to run simulations with real-time constraints, and extending the paradigm for actual real-time systems. Augmented the Time-Warp discrete-event simulation testbed (referred to above) to incorporate real-time constraints and pursue the implications of performing speculative computations in time-constrained systems, and using rollback-synchronization in such systems. (Testbed implemented on the Butterfly and the KSR multiprocessors.)
  - Designed and implemented an abstraction called 'carriers' to investigate the dependence between reliability and cost of message passing for applications with dynamic communication patterns running on multicomputers. (Implemented on the Butterfly multiprocessor, and an in-house architecture at Georgia Tech (part of the SPOCK project), consisting of a network of microprocessors.)
  - Benchmarking of real-time systems. Investigating the effects of communication latencies, and processing at the sender and receiver for real-time applications with soft and hard deadlines. Sample applications implemented include processing of video data, and compression/decompression of said data. PVM used for the communication part, though any message-passing library can be 'plugged in.' (Implemented on a network of workstations.)
- 01/90 - 06/90: Teaching Assistant (Data Structures and Algorithms).
- 09/89 - 12/89 and 06/90 - 09/90: Systems Support. User-assistance and technical support for workstations, printers, and networking at the College of Computing.

Publications

- "Communication Across Fault-Containment Firewalls on the SGI Origin"
  Kaushik Ghosh and Allan J. Christie.
  In *Proceedings of the IEEE High Performance Computer Architecture Symposium*, February 1998.

- "Evaluating the Limits of Message Passing via the Shared Attraction Memory on CC-COMA Machines: Experiences with TCGMSG and PVM"
  Kaushik Ghosh and Stephen R. Breit.
  In *Proceedings of the International Conference on Supercomputing*, May 1996.

- "Reconfigurable Garbage-Collection of Data Structures in a Speculative Real-Time System"
  Kaushik Ghosh.
  Technical Report GIT-CC-94-57; submitted for publication.

- "PORTS: Experiences with a Scheduler for Dynamic Real-Time Systems"
  Kaushik Ghosh, Richard M. Fujimoto and Karsten Schwan.
  Extended abstract, technical report GIT-CC-94-29; submitted for publication.

- "PORTS: A Parallel, Optimistic, Real-Time Simulator"
  Kaushik Ghosh, Kiran Panesar, Richard M. Fujimoto and Karsten Schwan.
  In *Proceedings of the 8th Workshop on Parallel and Distributed Simulation (PADS)*, July 1994.

- "A Survey of Real-Time Operating Systems Concepts"
  Kaushik Ghosh, Bodhisattwa Mukherjee and Karsten Schwan.
  Draft (technical-report GIT-CC-93-18) available to Internet community.

- "A Machine Independent Interface for Lightweight Threads"
  Bodhisattwa Mukherjee, Greg Eisenhauer and Kaushik Ghosh.
  In *Operating Systems Review of ACM SIGOPS, Vol 28, Number 1* (January 1994).

- "Experimentation with Configurable, Lightweight Threads on a KSR Multiprocessor"
  Kaushik Ghosh, Bodhisattwa Mukherjee and Karsten Schwan.
  In *Proceedings of the First International Workshop on Parallel Processing*,Bangalore, India, December 1994. Extended version available as *Technical Report Number GIT-CC-93/37.*

- "Time Warp Simulation in Time-Constrained Systems"
  Kaushik Ghosh, Richard M. Fujimoto and Karsten Schwan.
  In *Proceedings of the 7th Workshop on Parallel and Distributed Simulation (PADS)*, May 1993.

- "A Testbed for Optimistic Execution of Real-Time Simulations"
  Kaushik Ghosh, Richard M. Fujimoto and Karsten Schwan.
  In *Proceedings of the IEEE Workshop on Parallel and Distributed Real-Time Systems*, in conjunction with the *7th International Parallel Processing Symposium*, April 1993.

- "Parallel Discrete-Event Simulation Using Space-Time Memory"
  Kaushik Ghosh and Richard M. Fujimoto.
  In *Proceedings of the 20th International Conference on Parallel Processing*, August 1991.

Awards

Jagadish Bose National Science Talent Search Award (through the undergraduate years).

Related Information, and Professional Activities

- Reviewed papers for the International Conference on Parallel Processing, Real Time Systems Symposium, International Conference on Distributed Computing Systems, IEEE Transactions on Software Engineering, IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Modeling and Computer Simulation, etc.
- Member of ACM (SIGOPS, SIGARCH, SIGCOMM, SIGMETRICS).

Visa Status

Permanent Resident of the US.