

# APARNA CHANDRAMOWLISHWARAN

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## EDUCATION

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**Georgia Institute of Technology**, Atlanta, GA

Ph.D., Computational Science and Engineering, 2008 – Present.

Advisor: Prof. Richard Vuduc.

**Georgia Institute of Technology**, Atlanta, GA

M.S., Computer Science, 2007 – Present.

Advisors: Prof. Richard Vuduc and Prof. David A. Bader.

GPA: 3.80/4.00.

**Anna University**, Chennai, India

B.Engg., Computer Science and Engineering, 2003 – 2007.

GPA: 8.3/10.0.

## RESEARCH INTERESTS

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Parallel Programming Models, Autotuning, Numerical and Discrete Algorithms in Computational Science.

## PROFESSIONAL EXPERIENCE

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**1. Georgia Institute of Technology**, Atlanta, GA.

Graduate Research Assistant, Computational Science and Engineering Division, Fall 2007 – Present.

Advisors: Prof. Richard Vuduc, Prof. David A. Bader.

**2. Lawrence Berkeley National Laboratory**, Berkeley, CA.

Intern, Future Technologies Group, Summer 2009. Advisor: Dr. Erich Strohmaier.

**3. Intel Corporation**, Hudson, MA.

Intern, Pathfinding and Innovation Division, Software Solutions Group, Summer 2008. Advisor: Dr. Kathleen Knobe.

**4. Tata Consultancy Services**, Hyderabad, India.

Intern, Advanced Technology Center, Summer 2007. Advisor: Dr. M. Vidyasagar.

## RESEARCH PROJECTS

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**1. Performance Optimization and Autotuning of the Fast Multipole Method**

Georgia Institute of Technology and LBNL, Fall 2008 – Present.

We are working on the performance optimization, tuning, and analysis of the kernel-independent fast multipole method (FMM) on modern multicore systems. The main feature of this FMM algorithm is that it does not require the implementation of multipole expansions of the underlying kernel, and is based only on kernel evaluations. We apply numerous performance enhancements to

both the single- and double-precision versions (low-level tuning, numerical approximation, data structure transformations, OpenMP parallelization, and algorithmic tuning). We also compare our single-precision code against prior state-of-the-art GPU-based code [Lashuk, Chandramowlishwaran, et al. (2009)] and show, surprisingly, that the most advanced cache-based multicore architecture (Nehalem) reaches parity in both performance and power efficiency with NVIDIA's most advanced GPU architecture.

## **2. Algorithm Design and Autotuning for the Concurrent Collections C/C++ Parallel Programming Model**

Georgia Institute of Technology and Intel Corporation, Summer 2008 – Present.

Intel Concurrent Collections (CnC) is a new programming model where the programmer just specifies high-level computational steps, including inputs and outputs, without imposing unnecessary ordering on their execution. This results in a separation of concerns between the specification of a program and the optimization of its execution on a target parallel architecture. We are investigating the use of CnC to design tuned numerical algorithms for emerging multicore architectures, capturing a mix of both highly asynchronous task-level parallelism and synchronous data parallelism. We have designed new asynchronous parallel implementations for Cholesky factorization and eigenvalue computation on dense matrices that outperform tuned parallel libraries on multi-core x86 platforms. We are also researching problems related to reuse and hierarchical representation of algorithmic steps in a CnC program, in the context of numerical kernel design.

## **3. Smart Prefetching Strategies for Multicore Architectures**

Georgia Institute of Technology, Fall 2008 – Present.

We are exploring several software prefetching optimizations for the sparse-matrix vector multiply kernel. We are experimenting with runtime prefetching parameter tuning, quantifying the gains for various input matrices, and working on a model for determining the best prefetch distance.

## **4. Accelerating Financial Applications on the Cell/B.E. processor**

Georgia Institute of Technology, Fall 2007 and Spring 2008.

The Cell/B.E. processor is a heterogeneous multicore architecture that offers a significant performance improvement over current architectures for data-intensive multimedia and scientific applications. We designed and optimized a parallel 64-bit pseudo-random number generator – a linear congruential generator (LCG) – for the Cell/B.E. Our LCG implementation achieves an average speedup of 33 over current Intel architectures. We use this fast generator for Monte Carlo simulations, and speed up the computation of Value at Risk (VaR), a commonly used model for risk assessment in financial markets.

## **5. Tunable Parallelism in the Asynchronous Variational Integrator (AVI) Framework**

Georgia Institute of Technology, Fall 2007.

The asynchronous variational integrator (AVI) framework by Lew et al. (Arch. Rational Mech. Anal. 2003) was originally developed for time-integration of partial differential equations (PDEs). We study tunable parallelism in the context of AVIs, by designing several multicore implementations. An AVI can be naturally cast as a discrete event simulation (DES), where element (or super-element) updates become events with prescribed time-stamps, and the DES software framework takes care of all the scheduling and causality-preserving details. We designed a scalable AVI implementation using the optimistic DES methodology, observing a speedup of nearly 30 on 64 threads of a Niagara 2 machine.

## 6. An Image-processing library for the Cell B./E. processor

Anna University, Fall 2006 and Spring 2007.

As part of my undergraduate senior year project, I designed an image-processing library for the Cell processor. The implementation included functions like convolution, laplacian filters, contrast stretching, thresholding, edge detection using MSB, Sobel edge detection, rotation and mirroring.

## 7. Indian Language Processing

Tata Consultancy Services, Summer 2006.

As a summer intern at Tata Consultancy Services, I worked on an automated converter for processing documents in Indian languages and standardizing them. This facilitates text processing operations like spell checking, searching, and sorting on the processed documents.

## PEER-REVIEWED PUBLICATIONS

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1. Ilya Lashuk, Aparna Chandramowliswaran, Harper Langston, Tuan-Anh Nguyen, Rahul Sam-path, Aashay Shringarpure, Richard Vuduc, Lexing Ying, Denis Zorin, and George Biros, "A massively parallel adaptive fast multipole method on heterogeneous architectures," *In Proc. ACM/IEEE Conf. Supercomputing (SC)*, Portland, OR, USA, November 2009. (to appear). **Best Paper Finalist.**

2. Zoran Budimlic, Aparna Chandramowliswaran, Kathleen Knobe, Geoff Lowney, Vivek Sarkar, Leo Treggiari, "Declarative Aspects of Memory Management in the Concurrent Collections Parallel Programming Model," *DAMP 2009: Workshop on Declarative Aspects of Multicore Programming*, Savannah, GA, January 20, 2009.

3. Zoran Budimlic, Aparna Chandramowliswaran, Kathleen Knobe, Geoff Lowney, Vivek Sarkar, Leo Treggiari, "Multi-core Implementations of the Concurrent Collections Programming Model," *The 14th Workshop on Compilers for Parallel Computing (CPC 2009)*, Zurich, Switzerland, January 7-9, 2009.

4. David A. Bader, Aparna Chandramowliswaran, Virat Agarwal, "On the Design of Fast Pseudo-Random Number Generators for the Cell Broadband Engine and an Application to Risk Analysis," *The 37th International Conference on Parallel Processing (ICPP 2008)*, Portland, OR, September 8-12, 2008.

5. Aparna Chandramowliswaran, Abhinav Karhu, Ketan Umare, Richard Vuduc, "Numerical Algorithms with Tunable Parallelism," *Third Workshop on Software Tools for MultiCore Systems (STMCS 2008)*, Boston, MA, April 6, 2008.

## POSTER PRESENTATIONS

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1. Aparna Chandramowliswaran, Kathleen Knobe, and Richard Vuduc, "Applying the Concurrent Collections Programming Model to Asynchronous Parallel Dense Linear Algebra," *In Proc. 15th ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming (PPoPP)*, Bangalore, India, January 2010. (peer-reviewed, to appear).

2. Aparna Chandramowliswaran, Multi-core Implementations of the Concurrent Collections Parallel Programming Model, " *CRA-W/CDC Programming Languages, Operating Systems, & Architecture Workshop (PLOSA)*," Washington, DC, March 2009.

3. Aparna Chandramowliswaran, Parallel Random Number Generation on the Cell Broadband Engine, " *SIAM Conference on Parallel Processing for Scientific Computing*," Atlanta, GA, March 12-

14, 2008.

## HONORS AND AWARDS

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1. *Student travel award*, The CRA-W Grad Cohort for Women Program, 2009.
2. *Student travel award*, PLOSA 2009: CRA-W/CDC Programming Languages, Operating Systems, and Architecture Workshop, 2009.
3. *Student volunteer award*, ACM Supercomputing 2008 Conference, 2008.
4. *Best all-round performer award*, Undergraduate class of Computer Science and Engineering students, 2007.

## GRADUATE CLASSES

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Numerical Approximation Theory, Computational Data Analysis, Numerical Linear Algebra, Parallel Numerical Algorithms, Discrete Algorithms in Computational Science and Engineering, High-Performance Computing: Tools and Applications, Parallel and Discrete Simulation, High Performance Computer Architecture.

## PROFESSIONAL ACTIVITIES

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1. External reviewer: The 37th International Conference on Parallel Processing (ICPP 2008), 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA 2008), The Second International Frontiers of Algorithmics Workshop (FAW 2008).
2. External reviewer: Journal for Parallel and Distributed Computing, 2008.
3. Student member, IEEE and SIAM.

## OTHER ACTIVITIES

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1. Team captain, Georgia Tech Women's table tennis team, 2007 - present.
2. Member, Women@CC (College of Computing) group, Georgia Tech, 2007 - present.
3. Fourth place, 2008 National Collegiate Table Tennis Association (NCTTA) Team Championship for Women.
4. Winner, NCTTA Southeast Conference Women Team Championship, 2008 and 2009.
5. Volunteered to teach Physics classes to high school students at Avon Institute of Modern Sciences, Chennai, India in 2006.
6. Sports scholarship for undergraduate studies, 2004-05.