

Fall 2004  
ECE 538  
Tu/Th 11:00am - 12:15pm  
Classroom: ECE Room 210

## **ECE 538: Advanced Computer Architecture**

<http://www.ece.unm.edu/~dbader/ece538/>

**Instructor:** Dr. David A. Bader, ECE 230B, 277-6724, [dbader@ece.unm.edu](mailto:dbader@ece.unm.edu)

**Course Assistant:** TBD

**Office Hours:** Tuesday/Thursday 10:00-10:45AM, or by appointment

**Textbook:** Hennessy and Patterson, *Computer Architecture: A Quantitative Approach, Third edition*, Morgan Kaufmann Publishers / Elsevier, 2002.

**Course Description:** Course provides an in-depth analysis of computer architecture techniques. Topics include high speed computing techniques, memory systems, pipelining, vector machines, parallel processing, multiprocessor systems, high-level language machines and data flow computers.

Prerequisites: Microprocessors.

### **Grading:**

- (20 %) Exam I
- (20 %) Exam II
- (25 %) Final
- (20 %) Design Project
- (10 %) Homework
- ( 5 %) Class participation

## **CLASS GOALS**

Computer architecture is a vibrant and ever changing field; this course will attempt to convey that to students. It focuses on the design and implementation of computer architectures, as well as techniques for analyzing and comparing alternative computer organizations. Students will learn about styles of computer implementation and organization from a historical and modern perspective. Traditional concepts such as pipelining, instruction-level parallelism, memory hierarchies, and input/output architectures will be discussed. Further, modern issues such as data speculation, dynamic compilation, communication architecture, and VLSI scaling concerns will be introduced and discussed.

## CLASS POLICIES

1. Class announcements will be sent to the **ECE538** mailing list. To subscribe, visit:  
<http://www.ece.unm.edu/mailman/listinfo/ece538/>.
2. **Exams.** Exams I, II, and Final will be in-class, closed-book exams. You will be allowed to take a “cheat sheet” (double-sided 8.5 x 11 sheet of paper) into each exam. The final exam is scheduled for Tuesday, December 14th, from 10am - 12pm.
3. Please let me know as soon as possible if you will need to re-schedule an exam, or have any special needs during the semester.

## Tentative Course Schedule

Week	Date	Lec	Topic	Read	HW assn	HW due
1	24 Aug	1	Syllabus; Review: Key abstractions	Ch. 1	1	
	26 Aug	2	Review: ISA, pipeline, hazards	Ch. 2		
2	31 Aug	3	Caches	5.1-5.7	2	1
	02 Sep	4	Memory Technology	5.8-5.18		
3	07 Sep	5	Storage Technology	7.1-7.6	3	2
	09 Sep	6	Cache wrapup			
4	14 Sep	7	Network Embedded Architecture		4	3
	16 Sep	8	Latency Tolerance and Multithreading			
5	21 Sep	9	Networks and NIs	8.1-8.7	5	4
	23 Sep	10	<b>Exam I</b>			
6	28 Sep	11	Micro Architecture - Hazards, Dynamic sched	3.1-3.3		
	30 Sep	12	Superscalar Processor Design: Techniques	3.4-3.15	6	5
7	05 Oct	13	ILP	3.4-3.9		
	07 Oct	14	SMT	3.10-3.12	7	6
8	12 Oct	15	Vector Processors			
	14 Oct	-	<i>Fall Break</i>			
9	19 Oct	16	Multiprocessors & CMT	6.1-6.4	8	7
	21 Oct	17	DSM and Availability	6.5-6.7		
10	26 Oct	18	Shared-memory multiprocessors	6.8-6.16		
	28 Oct	19	Distributed-memory systems	8.10-8.12		8
11	02 Nov	20	<b>Exam II</b>			
	04 Nov	21	Massively Parallel Processors			
12	09 Nov	22	TBD			
	11 Nov	23	TBD			
13	16 Nov	24	High-productivity computing systems			
	18 Nov	25	IBM PERCS, Cray Cascade, Sun HERO			
14	23 Nov	26	Terascale systems			
	25 Nov	27	<i>Thanksgiving Holiday</i>			
15	30 Nov	28	Near-memory processing, PIM			
	02 Dec	29	Reconfigurable architectures			
16	07 Dec	30	Student presentations			
	09 Dec	31	Student presentations			
17	14 Dec	-	<b>Final Exam</b> (10am-12pm)			