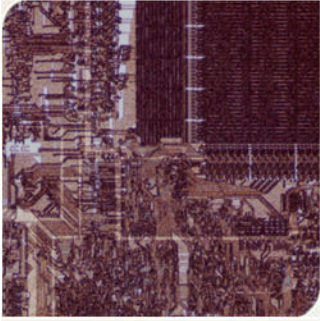


# CS 6290 HPCA

Fall 2009

Prof. Hyesoon Kim



**Georgia  
Tech**



College of  
Computing

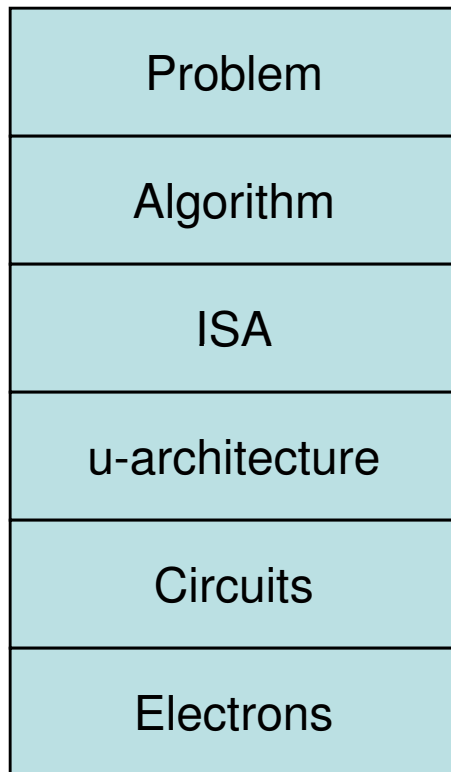


# Class Info

- Instructor: Hyesoon Kim (KACB 2344)
  - Email: [hyesoon@cc.gatech.edu](mailto:hyesoon@cc.gatech.edu)
- Homepage
  - <http://www.cc.gatech.edu/~hyesoon/fall09>
  - T-square (<http://www.t-square.gatech.edu>)
- Office hours: 3:00-4:00 Tu/TH
- TA: TBA
- Textbook:
  - Computer Architecture: AQA, **4<sup>th</sup> Edition**  
by Hennessy and Patterson  
Papers



# What is Architecture?



ISA: Interface between s/w & h/w



# ISA (Instruction Set Architecture)

- Opcode
- Data type
- Addressing mode: register, immediate, displacement
  - E.g.) x86 SIB
- Memory addressing: unaligned, aligned



# What is Architecture?

- Original sense:
  - Taking a range of building materials, putting together in desirable ways to achieve a building suited to its purpose
- In Computer Science:
  - Similar: how parts are put together to achieve some overall goal
  - Examples: the architecture of a chip, of the Internet, of an enterprise database system, an email system, a cable TV distribution system

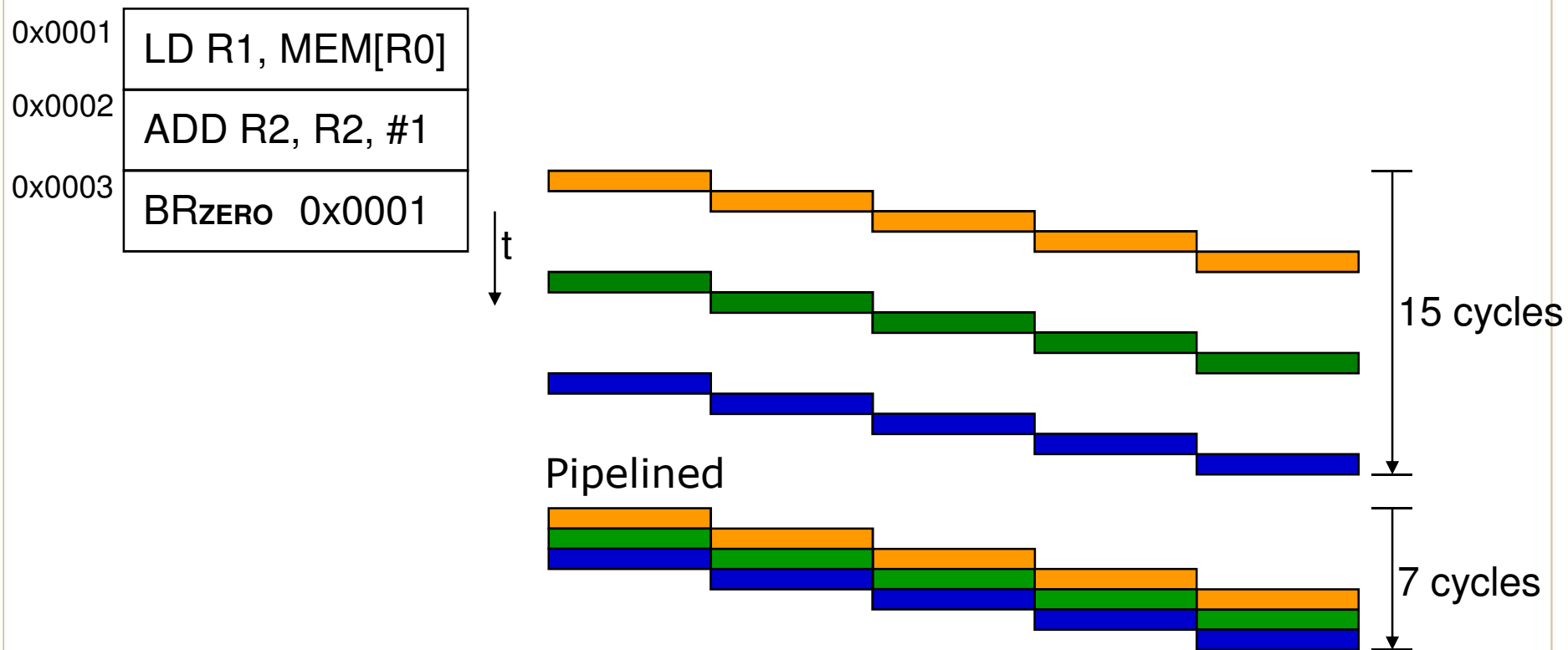


# Why Computer Architecture?

- Exploit advances in technology
  - Make things Faster, Smaller, Cheaper, ...
- Which enables new applications
  - Life-like 3D games 15 years ago?
- Make new things possible
  - Smart dust? Accurate one-month weather forecasts? Cure for cancer?
- The advancement of computer architecture is vital for the advancement of all other areas of computing!

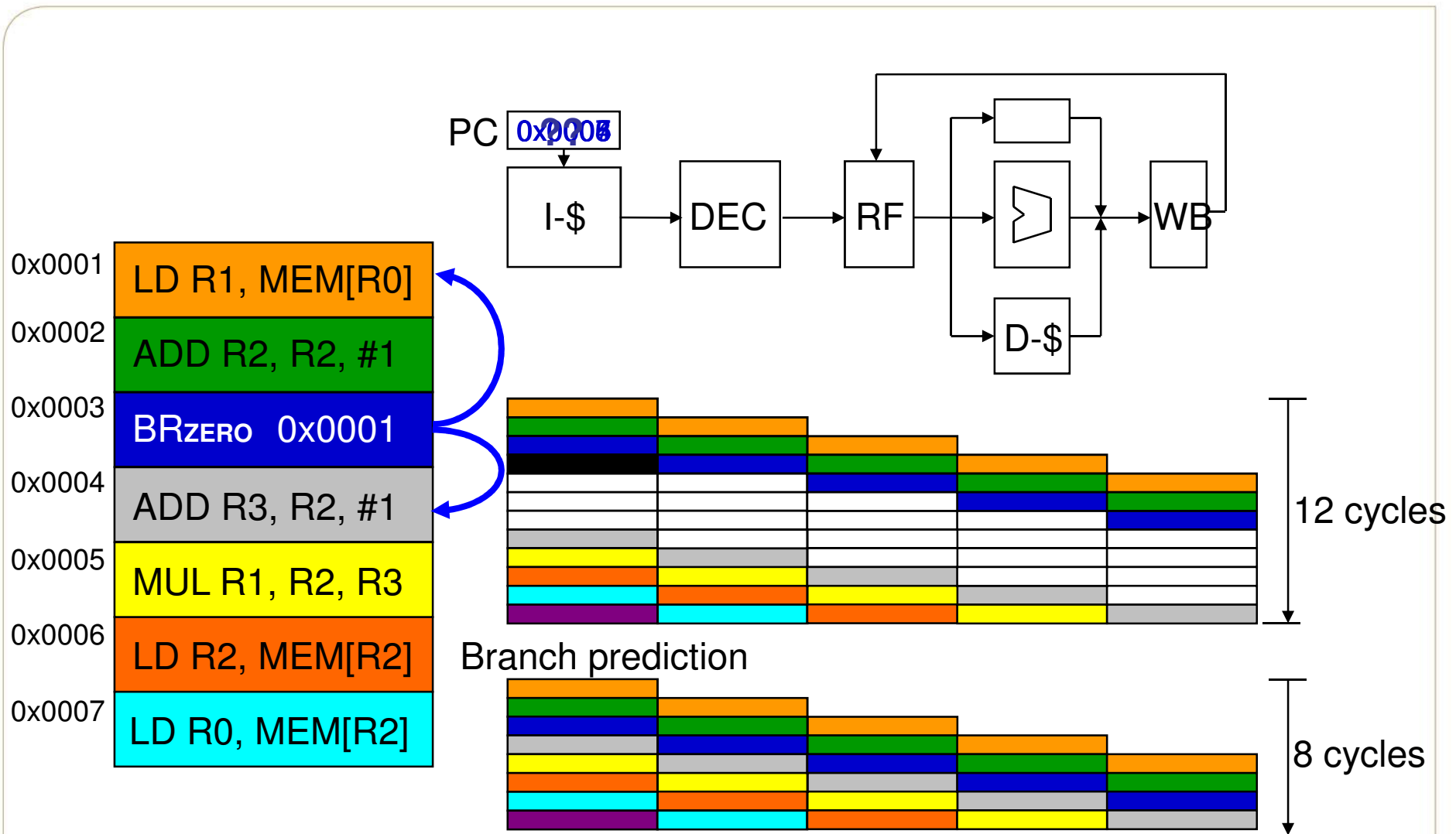


# Overview of a Processor

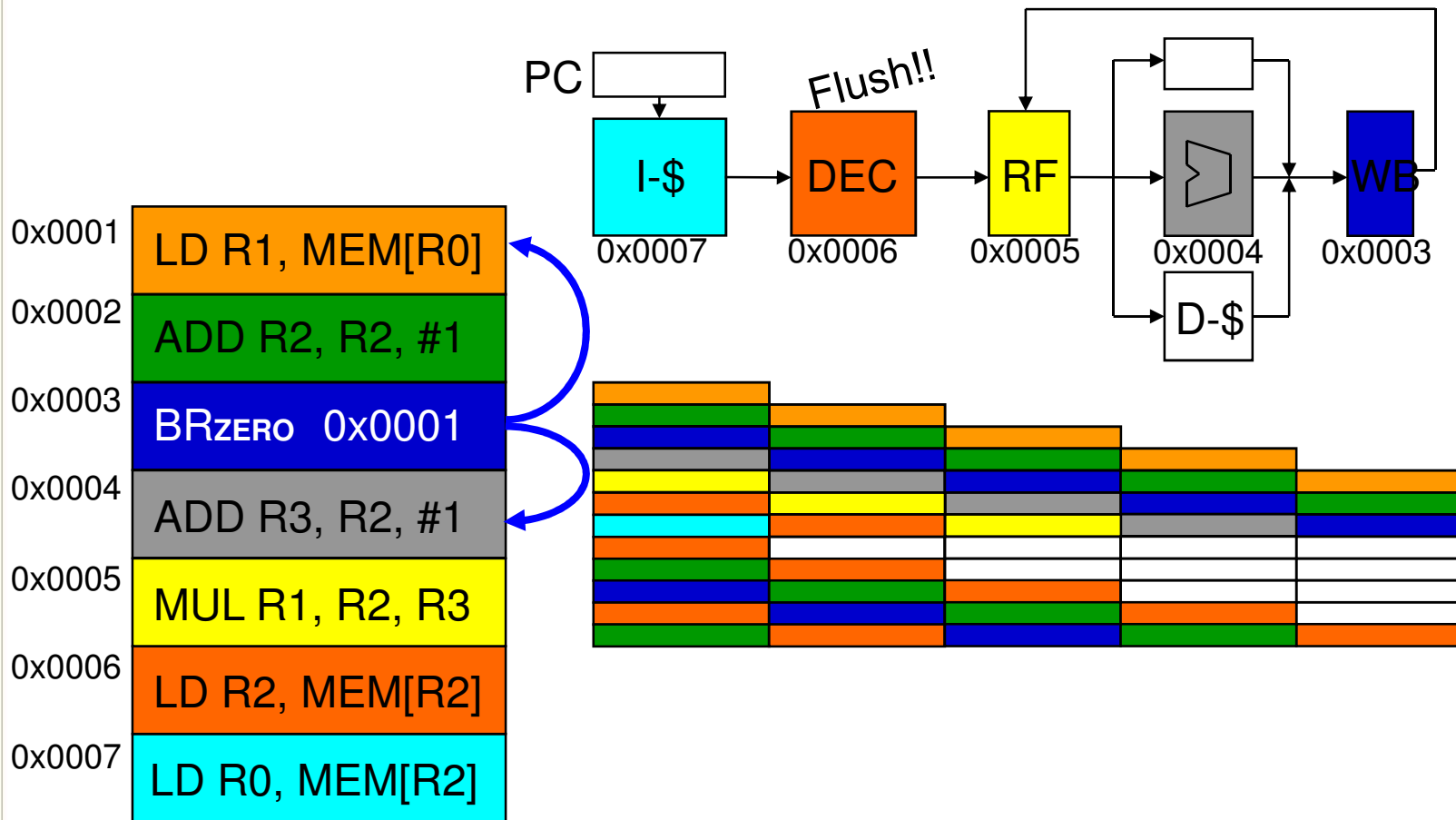


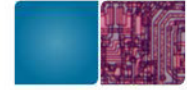


# What To Fetch Next?



# Misprediction Penalty





# In this Course

Branch predictor algorithms

Dynamic instruction scheduling (OOO)

Cache, memory, memory schedulers

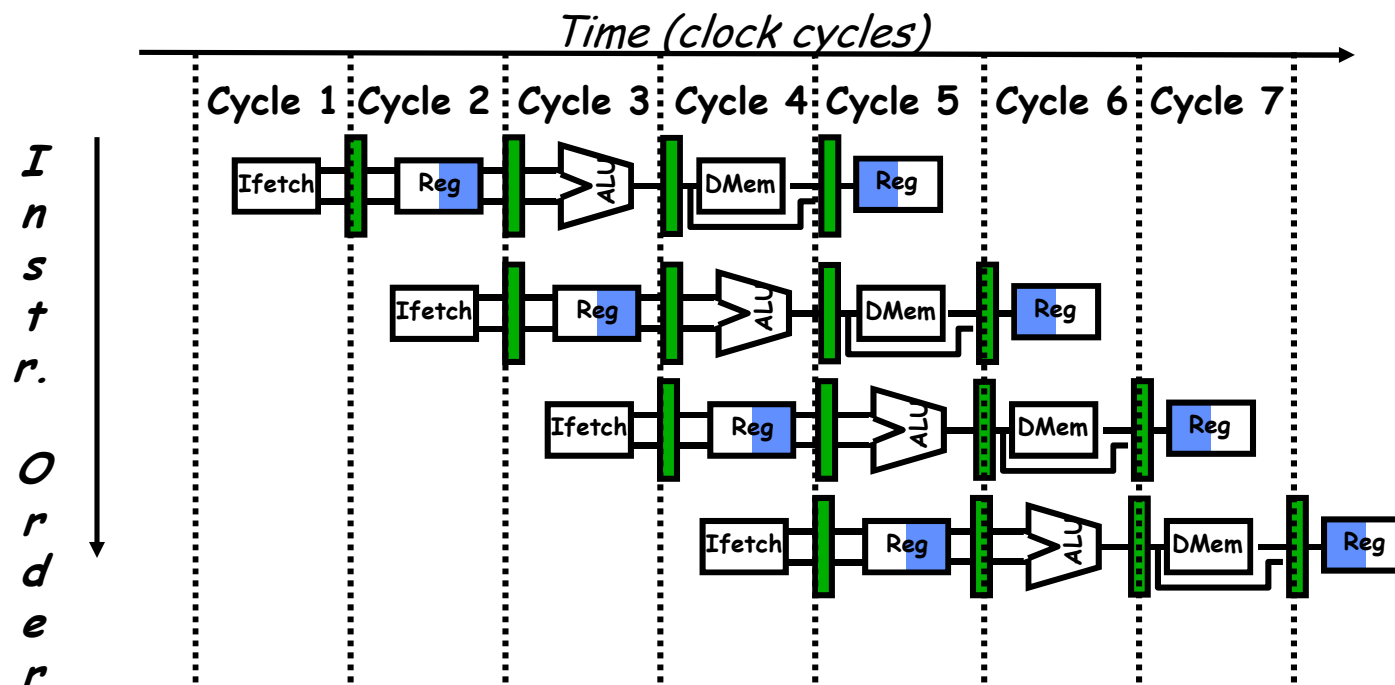
Multi processors, SMT

Power

Storage and interconnect

Case studies on modern processors and  
graphics processors

# Basic Pipeline



Instructions issued in order

Operand fetch is stage 2 => operand fetched in order

Write back in stage 5 => no WAW, no WAR hazards

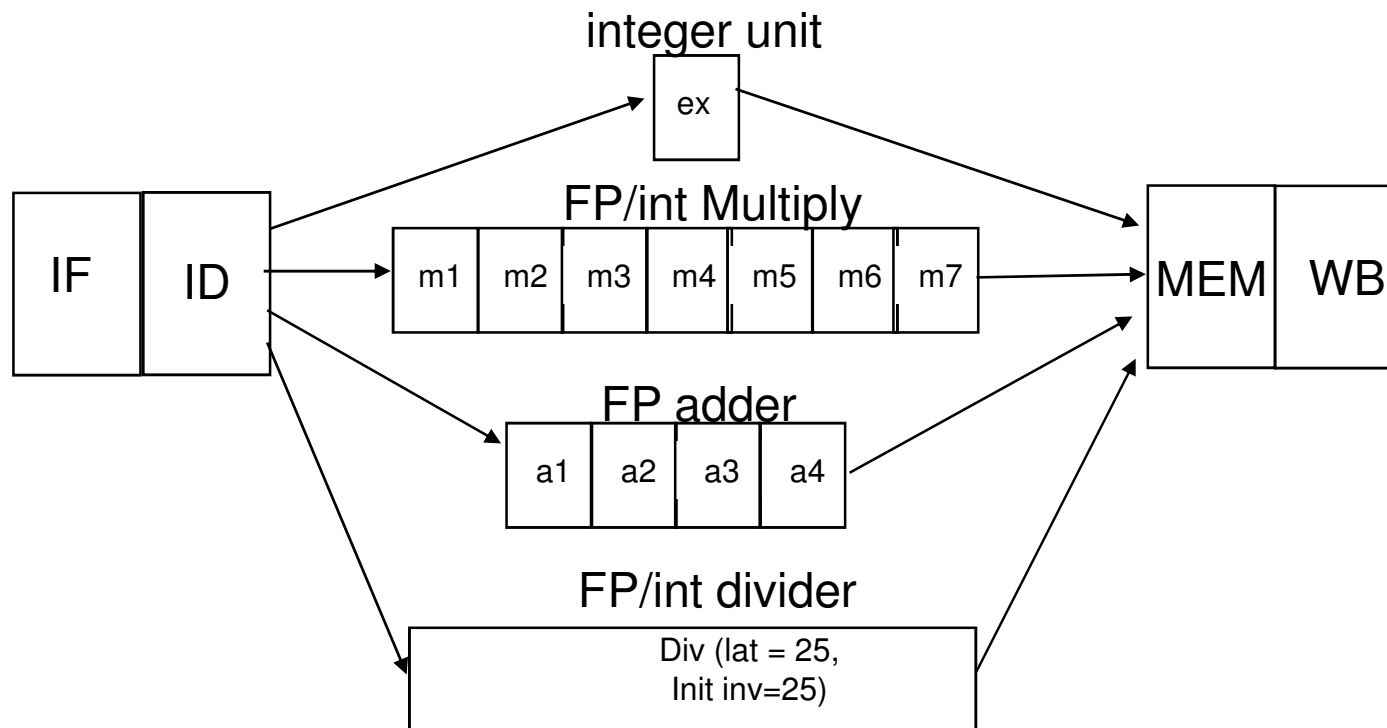
Common pipeline flow => operands complete in order

Stage changes only at "end of instruction"



# Multicycle stages

## Example: MIPS R4000





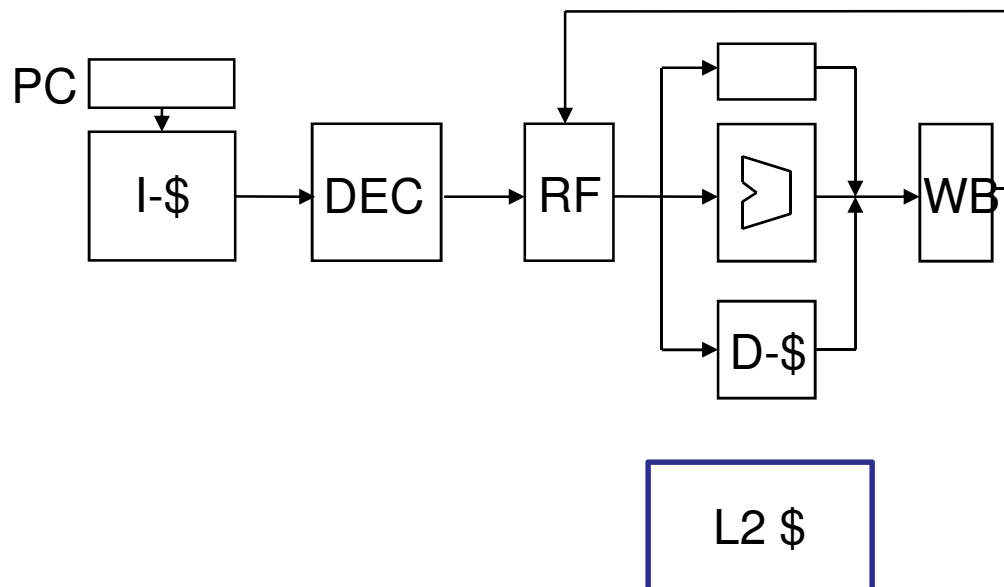
# Trace driven vs. Execution driven

- Trace driven: instructions are all executed
  - Easy to develop a simulator
  - Could be faster to simulate
  - Our lab assignment
- Execution driven: simulator executes instructions during simulation time.
  - Development time is longer.
  - Can simulate wrong-path instructions, multi thread instruction behavior



# Programming Assignments

- Lab #1: Build a cycle accurate simulator
  - Design and Implement a pipelined processor
  - In-order processor





# Programming Assignments

- Lab #2: Improve the cycle accurate simulator
  - Out of order processor
  - Branch predictor
    - (Speculative execution, register renaming)



# Programming Assignments

- Lab #3: Supporting multiprocessor architecture
  - Change the cache structures
  - Implement multiple L2 caches.
  - Implement a hardware prefetcher



# Project Option

- Instead of programming assignment #2, #3, you can do a research project
- Combine with your own research area
- Projects can lead to a paper
- Can be continued with CS8903 next semester
  - ISCA (due middle Nov. ) : France!!
  - DAC (due middle Dec)
  - DSN (due middle Dec. )
  - ISC (due middle Jan )
  - MICRO (due next year May):: Here Atlanta!