

**Gabriel H. Loh**  
**Assistant Professor**  
**College of Computing**  
**Georgia Institute of Technology**  
**Atlanta, Georgia 30332-0765**  
loh@cc.gatech.edu  
<http://www.cc.gatech.edu/~loh/>

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## EDUCATIONAL BACKGROUND

<b>Degree</b>	<b>Year</b>	<b>University</b>	<b>Field</b>
Ph.D.	2002	Yale University	Computer Science
M.S.	1999	Yale University	Computer Science
B.Eng.	1998	The Cooper Union	Electrical Engineering

## EMPLOYMENT HISTORY

<b>Title</b>	<b>Organization</b>	<b>Years</b>
<b>Assistant Professor</b>	College of Computing Georgia Institute of Technology	8/2004–present
<b>Senior Researcher</b>	Microarchitecture Research Laboratory Corporate Technologies Group Intel Corporation	7/2003–7/2004
<b>Research and Teaching Assistant</b>	Department of Computer Science Yale University	9/1998–12/2002
<b>Research Intern</b>	Performance Analysis Group Akamai Technologies	5/2000–10/2000

## CURRENT FIELDS OF INTEREST

### **Computer Microarchitecture**

My main research interest is the design of new microprocessor organizations for maximizing the potential of new fabrication technologies. Three-dimensional die-stacking integration technology will soon be available for the design of high-performance microprocessors. While there has been considerable research in materials and packaging for 3D, there is currently little to no research in how a processor architect would actually make use of this new technology in the design of new CPUs. My current research efforts are focused on filling this void. I am currently studying how the technology impacts conventional microprocessor design.

Before high-performance 3D-integrated processors become a reality, the computer architecture community must still make progress in conventional processor design. In this area, the research problem that I am focused on is finding new techniques and methods to reduce power consumption and design complexity while simultaneously continuing to improve performance. I have on-going projects targeting a variety of processor topics including caching, branch prediction, and dynamic instruction scheduling and execution.

## I. TEACHING

### A. Courses Taught

<u>Semester/Year</u>	<u>Course</u>	<u>Class Size</u>	<u>Teaching Effectiveness</u>	<u>Comments</u>
Fall 2008	CS3220 Processor Design	29	—	Major revision
Spring 2008	CS6290-RKR High-Performance Computer Architecture	29	5.0	GT MSCS Korea Program <sup>†</sup>
Spring 2008	CS6290-A High-Performance Computer Architecture	32	5.0	
Spring 2008	CS8803AMA Advanced Microarchitecture	10	5.0	
Fall 2007	CS8001CAS Computer Architecture Seminar	23	—	
Spring 2007	CS4290/6290 High-Performance Computer Architecture	17	4.7	GT MSCS Korea Program <sup>‡</sup>
Fall 2006	CS4290/6290 High-Performance Computer Architecture	48	4.8	
Fall 2006	CS8001CAS Computer Architecture Seminar	11	—	
Spring 2006	CS4290/6290 High-Performance Computer Architecture	51	4.8	*
Fall 2005	CS8803AMA Advanced Microarchitecture	14	5.0	New Course
Spring 2005	CS3220 Processor Design	9	4.2	
Fall 2001	Advanced Computer Architecture	18	n/a	At the Cooper Union

<sup>†</sup>29 students in the Korea (RKR) section, 32 in Atlanta (A); separate course surveys were given.

<sup>‡</sup>Taught on location in Seoul, South Korea.

\*Received CETL “Thank a Teacher” recognition.

### B. Continuing Education

None.

### C. Curriculum Development

CS 8803AMA: Advanced Microarchitecture. Prior to this course, computer architecture students had no advanced classes to take beyond the introductory CS6290 offering. This course fills a void in the computer architecture course offerings providing coverage of advanced topics in the microarchitecture of modern (and future) processor designs. The curriculum combines a lecture-based, in-depth exploration of modern superscalar, dynamically scheduled processors with discussion-based case studies of real processor designs. This course has not been offered twice, and I will now apply to have the course promoted to a regularly offered 7000-level course.

### D. Individual Student Guidance

#### 1. Research Scientists Supervised

None.

#### 2. Ph.D. Students Supervised

**Guanhao Shen (CoC):** Fall 2008-Present

**Yuejian Xie (CoC):** Fall 2007-Present

**Samantika Subramaniam (CoC):** Fall 2006-Present

**Kiran Puttaswamy (ECE):** Fall 2004-December 2007, thesis: Designing High-Performance Microprocessors in 3-Dimensional Integration Technology

**Brad Nemanich (CoC):** Spring 2005-Summer 2005

3. Ph.D. Special Problems Students

None.

4. M.S. Special Problems Students

**Samantika Subramaniam (CoC):** Spring 2005-Summer 2006

Examining Timeliness in the Design of Hardware Predictors for Memory-Ordering Violations

**Sarang Karandikar (CoC):** Spring 2006

Evaluating the Architectural Impact of Probabilistic Instruction Execution

**Zain Chandra (CoC):** Fall 2005

Evaluating the Impact of Steering Algorithms on Clustered Microarchitectures

**Ranjith Subramanian (CoC):** Fall 2005-Spring 2007 (co-advised with Yannis Smaragdakis)

Hybrid Cache Replacement Policies to Counteract Pathological Access Patterns

**Rahul Garde (CoC):** Fall 2006-Spring 2008

Adaptive Cache Replacement Policies for Multi-Core Processors

**Kedar Karandikar (ECE):** Fall 2008

Explaining and Exploiting Holes in Branch Correlation

5. Undergraduate Special Problems Students

**Sashmit Bhaduri:** Fall 2005-present

A Generalization of Correlation-Based Branch Prediction and the Use of Genetic Algorithms for their Optimization. **2006 UROC Symposium 3rd place Judge's Award**

**Luke Snyder:** Fall 2004-Spring 2005

A New Cache Design through Intelligent Use of Memory Reference Behavior. **2005 UROC Symposium 3rd place Judge's Award and 3rd place People's Choice Award.**

**Matt Wood:** Fall 2004-Spring 2005

Design of Efficient Branch Predictors Using State-Subsetting of Neural Algorithms.

**E. Teaching Honors and Awards**

None.

## **II. RESEARCH AND CREATIVE SCHOLARSHIP**

### **A. Theses**

#### **Ph.D. Thesis**

Microarchitecture for Billion-Transistor VLSI Superscalar Processors

Date Completed: December 2002

Adviser: Dana S. Henry

University: Yale University

### **B. Journal Articles (refereed)**

#### **B.1. Published Journal Articles (refereed)**

1. Bradley C. Kuszmaul, Dana S. Henry, Gabriel H. Loh. A Comparison of Asymptotically Scalable Superscalar Processors. In the *Theory of Computing Systems*, Springer, volume 35(2), pages 129–150, 2002.
2. Gabriel H. Loh, Dana S. Henry, Arvind Krishnamurthy. Exploiting Bias in the Hysteresis Bit of 2-bit Saturating Counters in Branch Predictors. In the *Journal of Instruction Level Parallelism*, volume 5, pages 1–32, 2003.
3. Gabriel H. Loh. Width-Partitioned Load Value Predictors. In the *Journal of Instruction Level Parallelism*, volume 5, pages 1–23, 2003.
4. Gabriel H. Loh. Deconstructing the Frankenpredictor for Implementable Branch Predictors. In the *Journal of Instruction Level Parallelism*, volume 7, pages 1–10, 2005.
5. Yuan Xie, Gabriel H. Loh, Bryan Black, Kerry Bernstein. Design Space Exploration for 3D Architectures. In the *ACM Journal of Emerging Technologies in Computing Systems*, volume 2(2), pages 65–103, April 2006.
6. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, Gabriel H. Loh. Multi-Objective Microarchitectural Floorplanning for 2D and 3D ICs. In the *IEEE Transactions on Computer Aided Design*, volume 26(1), pages 38–52, January 2007.
7. Gabriel H. Loh, Yuan Xie, Bryan Black. Processor Design in Three-Dimensional Die-Stacking Technologies. In *IEEE Micro*, volume 27(3), pages 31–48, May/June 2007.
8. Peter G. Sassone, D. Scott Wills, Gabriel H. Loh. Static Strands: Safely Exposing Dependence Chains for Increasing Embedded Power Efficiency. In the *ACM Transactions on Embedded Computing Systems*, September 2007.
9. Daniel Jiménez, Gabriel H. Loh. Modulo Path History for the Reduction of Pipeline Overheads in Path-Based Neural Branch Predictors. In the *International Journal of Parallel Programming*, Springer, January, 2008.
10. Kiran Puttaswamy, Gabriel H. Loh. 3D-integrated SRAM Components for High-Performance Microprocessors. To appear in *IEEE Transactions on Computers*.

#### **B.2. Articles Under Review (refereed)**

1. Samantika Subramaniam, Gabriel H. Loh. Design and Optimization of the Store Vectors Memory Dependence Predictor. Submitted to the *ACM Transactions on Architecture and Code Optimization*.
2. Kiran Puttaswamy, Gabriel H. Loh. High-Performance, Efficient and Scalable 3D-Integrated Arithmetic Units. Submitted to the *IEEE Transactions on VLSI*.

### **C. Published Books and Parts of Books**

1. Gabriel H. Loh. Advanced Instruction Flow Techniques. In John Paul Shen and Mikko Lipasti, *Modern Processor Design: Fundamentals of Superscalar Processors*. McGraw Hill, 2005.

## D. Conference Presentations

### D.1. Conference Presentations with Proceedings (refereed)

1. Bradley C. Kuszmaul, Dana S. Henry, Gabriel H. Loh. A Comparison of Scalable Superscalar Processors. In the *Proceedings of the ACM Symposium on Parallel Algorithms and Architectures–SPAA*, pages 126–137, June 1999.
2. Dana S. Henry, Bradley C. Kuszmaul, Gabriel H. Loh, Rahul Sami. Circuits for Wide-Window Superscalar Processors. In the *Proceedings of the ACM International Symposium on Computer Architecture–ISCA*, pages 226–247, June 2000. (Acceptance Rate: 17%)
3. Gabriel H. Loh. A Time-Stamping Algorithm for Efficient Performance Estimation of Superscalar Processors. In the *Proceedings of the ACM International Conference on Measurement and Modeling of Computer Systems–SIGMETRICS*, pages 72–81, June 2001. (Acceptance Rate: 12%)
4. Dana S. Henry, Gabriel H. Loh, Rahul Sami. Speculative Clustered Caches for Clustered Processors. In the *Proceedings of the International Symposium on High Performance Computing–ISHPC*, pages 281–290, May 2002.
5. Gabriel H. Loh, Dana S. Henry. Applying Machine Learning for Ensemble Branch Predictors. In the *Proceedings of the Conference on Industrial and Engineering Applications of Artificial Intelligence and Expert Systems*, pages 264–274, June 2002. (Best paper nominee.)
6. Gabriel H. Loh, Dana S. Henry. Predicting Conditional Branches with Fusion-Based Hybrid Predictors. In the *Proceedings of the ACM Conference on Parallel Architecture and Compilation Techniques–PACT*, pages 165–176, September 2002. (Acceptance Rate: 21%)
7. Gabriel H. Loh. Exploiting Data-Width Locality to Increase Superscalar Execution Bandwidth. In the *Proceedings of the IEEE International Symposium on Microarchitecture–MICRO*, pages 395–405, November 2002. (Acceptance rate: 24%)
8. Gabriel H. Loh. Simulation Differences Between Academia and Industry: A Branch Prediction Case Study. In the *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software–ISPASS*, pages 21–31, March 2005.
9. Peter G. Sassone, D. Scott Wills, Gabriel H. Loh. Static Strands: Safely Exposing Dependence Chains for increasing Embedded Power Efficiency. In the *Proceedings of the ACM Conference on Languages, Compilers and Tools for Embedded Systems–LCTES*, pages 127–136, June 2005.
10. Gabriel H. Loh. A Simple Divide-and-Conquer Approach for Neural-Class Branch Prediction. In the *Proceedings of the ACM International Conference on Parallel Architectures and Compilation Techniques–PACT*, pages 243–254, September 2005. (Acceptance Rate: 25%)
11. Kiran Puttaswamy, Gabriel H. Loh. Implementing Caches in a 3D Technology for High Performance Processors. In the *Proceedings of the IEEE International Conference on Computer Design–ICCD*, pages 525–532, October 2005.
12. Samantika Subramaniam, Gabriel H. Loh. Store Vectors for Scalable Memory Dependence Prediction and Scheduling. In the *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture–HPCA*, pages 64–75, February 2006. (**Best student presentation award**, Acceptance Rate: 14%)
13. Michael Healy, Mario Vites, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, Gabriel H. Loh. Microarchitectural Floorplanning Under Performance and Temperature Tradeoff. In the *Proceedings of Design, Automation and Test in Europe–DATE*, pages 1288–1293, March 2006.
14. Kiran Puttaswamy, Gabriel H. Loh. Implementing Register Files for High-Performance Microprocessors in a Die-Stacked (3D) Technology. In the *Proceedings of the IEEE International Symposium on VLSI–ISVLSI*, pages 384–389, March 2006.

15. Gabriel H. Loh. Revisiting the Performance Impact of Branch Predictor Latencies. In the *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software–ISPASS*, pages 59–69, March 2006.
16. Kiran Puttaswamy, Gabriel H. Loh. Thermal Analysis of a 3D Die-Stacked High-Performance Microprocessor. In the *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI–GLSVLSI*, pages 19–24, May 2006.
17. Kiran Puttaswamy, Gabriel H. Loh. Dynamic Instruction Schedulers in a 3-Dimensional Integration Technology. In the *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI–GLSVLSI*, pages 153–158, May 2006.
18. Kiran Puttaswamy, Gabriel H. Loh. The Impact of 3-Dimensional Integration on the Design of Arithmetic Units. In the *Proceedings of the IEEE International Symposium on Circuits and Systems–ISCAS*, pages 4951–4954, May 2006.
19. Daniel A. Jiménez, Gabriel H. Loh. Controlling the Power and Area of Neural Branch Predictors for Practical Implementation in High-Performance Processors. In the *Proceedings of the IEEE International Symposium on Computer Architecture and High Performance Computing–SBAC-PAD*, pages 55–62, October 2006. (Acceptance Rate: 23%)
20. Chinnakrishnan Ballapuram and Kiran Puttaswamy and Gabriel H. Loh and Hsien-Hsin S. Lee. Entropy-based Low Power Data TLB Design. In the *Proceedings of the ACM/IEEE International Conference on Compilers, Architecture and Synthesis for Embedded Systems–CASES*, pages 304–311, October 2006.
21. Samantika Subramaniam, Gabriel H. Loh. Fire-and-Forget: Load/Store Scheduling with No Store Queue at All. In the *Proceedings of the IEEE International Symposium on Microarchitecture–MICRO*, pages 273–284, December 2006. (**Best student presentation award**, Acceptance Rate: 24%)
22. Ranjith Subramanian, Yannis Smaragdakis, Gabriel H. Loh. Adaptive Caches: Effective Shaping of Cache Behavior to Workloads. In the *Proceedings of the IEEE International Symposium on Microarchitecture–MICRO*, pages 385–396, December 2006. (**Best paper nominee**, Acceptance Rate: 24%)
23. Bryan Black, Edward Brekelbaum, John DeVale, Gabriel H. Loh, Don McCauley, Pat Morrow, Don Nelson, Daniel Pantuso, Paul Reed, Jeff Rupley, Sadas Shankar, John Paul Shen, Clair Webb. Die Stacking (3D) Microarchitecture. In the *Proceedings of the IEEE International Symposium on Microarchitecture–MICRO*, pages 469–479, December 2006. (Acceptance Rate: 24%)
24. Kiran Puttaswamy, Gabriel H. Loh. Thermal Herding: Microarchitecture Techniques for Controlling HotSpots in High-Performance 3D-Integrated Processors. In the *Proceedings of the IEEE International Symposium on High Performance Computer Architecture–HPCA*, pages 193–204, February 2007. (Acceptance Rate: 16%)
25. Kiran Puttaswamy, Gabriel H. Loh. Scalability of 3D-Integrated Arithmetic Units in High-Performance Microprocessors. In the *Proceedings of the ACM Design Automation Conference–DAC*, pages 622–625, June 2007. (Acceptance Rate: 23%)
26. Peter G. Sassone, Jeff Rupley, Edward Brekelbaum, Gabriel H. Loh, Bryan Black. Matrix Scheduler Reloaded. In the *Proceedings of the ACM International Symposium on Computer Architecture–ISCA*, pages 335–346, June 2007. (Acceptance Rate: 23%)
27. Samantika Subramaniam, Milos Prvulovic, Gabriel H. Loh. PEEP: Exploiting Predictability of Memory Dependences in SMT Processors. In the *Proceedings of the 18th ACM/IEEE International Symposium on High-Performance Computer Architecture–HPCA*, pages 267–286, February 2008. (Acceptance Rate: 20%)
28. Gabriel H. Loh. A Modular 3D Processor for Flexible Product Design and Technology Migration. In the *Proceedings of the ACM International Conference on Computing Frontiers*, pages 159–170, May 2008.
29. Gabriel H. Loh. 3D-Stacked Memory Architectures for Multi-Core Processors. In the *Proceedings of the ACM International Symposium on Computer Architecture–ISCA*, pages 453–464, June 2008. (Acceptance Rate: 13%)

30. Mauricio Breternitz Jr., Gabriel H. Loh, Bryan Black, Jeff Rupley, Peter G. Sassone, Wesley Attrot, Youfeng Wu. A Segmented Bloom Filter Algorithm for Efficient Predictors. To appear in the *Proceedings of the IEEE International Symposium on Computer Architecture and High Performance Computing–SBAC-PAD*, October 2008.
31. Michael B. Healy, Hsien-Hsin S. Lee, Gabriel H. Loh, Sung Kyu Lim. Thermal Optimization in Multi-Granularity Multi-Core Floorplanning. To appear in the *Proceedings of the Asia South Pacific Design Automation Conference–ASPDAC*, January 2009.

#### **D.2. Workshop Publications (refereed)**

1. Gabriel H. Loh, Rahul Sami, Daniel H. Friendly. Memory Bypassing: Not Worth the Effort. In *Proceedings of the 1st Workshop on Duplicating, Deconstructing and Debunking–WDDD*, pages 71–80, May 2002.
2. Gabriel H. Loh. Width Prediction for Reducing Value Predictor Size and Power. In *Proceedings of the 1st Value Prediction Workshop*, pages 86–93, June 2003.
3. Gabriel H. Loh. The Frankenpredictor: Stitching Together Nasty Bits of Other Branch Predictors. In *Proceedings of the 1st Championship Branch Predictor Competition*, December 2004.
4. Gabriel H. Loh, Daniel A. Jiménez. Reducing the Power and Complexity of Path-Based Neural Branch Prediction. In *Proceedings of the 5th Workshop on Complexity Effective Design*, June 2005.
5. Rahul Garde, Samantika Subramaniam, Gabriel H. Loh. Deconstructing the Inefficacy of Global Cache Replacement Policies. In *Proceedings of the 7th Workshop on Duplicating, Deconstructing and Debunking–WDDD*, June 2008.
6. Yuejian Xie, Gabriel H. Loh. Dynamic Classification of Program Memory Behaviors in CMPs. In *Proceedings of the 2nd Workshop on Chip Multiprocessor Memory Systems and Interconnects–CMP-MSI*, June 2008.
7. Jonathan D. Kron, Brooks Prumo, Gabriel H. Loh. Double-DIP: Augmenting DIP with Adaptive Promotion Policies to Manage Shared L2 Caches. In *Proceedings of the 2nd Workshop on Chip Multiprocessor Memory Systems and Interconnects–CMP-MSI*, June 2008.
8. Gabriel H. Loh. The Cost of Uncore in Throughput-Oriented Many-Core Processors. In *Proceedings of the Workshop on Architectures and Languages for Throughput Applications–ALTA*, June 2008.

#### **D.3. Other Publications (refereed)**

1. Samantika Subramaniam, Gabriel H. Loh. Exploiting Predictability in Memory Dependences to Mitigate Load Latencies (poster). In the *Grace Hopper Celebration for Women in Computing Conference*, October 2007.

#### **E. Research Proposals and Grants (Principal Investigator)**

##### **a. Approved and Funded**

1. **High-Efficiency High-Performance Microarchitecture**  
Intel Corporation  
2004: Funded \$22,500, plus ≈\$65,000 in equipment  
2005: Funded \$27,310  
2006: Funded \$27,310
2. **High-Performance 3D Microarchitecture Design**  
Co-PIs: Hsien-Hsin S. Lee (ECE), Sung Kyu Lim (ECE)  
MARCO Microarchitecture Thrust  
2005: Funded \$60,000  
2006: Funded \$156,000  
2007-2009: Funded ≈\$150,000 per year

3. **CAREER: Computer Architecture Foundations for 3D-Integrated High-Performance Microprocessors**  
April 2007  
National Science Foundation  
Requested: \$449,999, Funded: \$400,000, GT Matching Funds: \$25,000

4. **CPA: Economic Mechanisms for Dynamic Resource Partitioning in Multi-Core Processors**  
September 2007  
National Science Foundation  
Requested: \$375,000, Funded: \$172,670

**b. Pending**

1. **II-NEW: A Flexible, Heterogeneous Testbed for Many-Core Research**  
Co-PIs: Nathan Clark, Thomas Conte, Hyesoon Kim, Milos Prvulovic  
September 2008  
National Science Foundation  
Requested: \$400,000

**c. Not Funded**

1. **CAREER: Leveraging Common-Case Behaviors for Power-Efficient High-Performance Microarchitectures**  
National Science Foundation  
Requested: \$450,000

**F. Research Proposals and Grants (Contributor)**

**a. Approved and Funded**

None.

**b. Pending**

1. **Design, Fabrication and Testing of 3D-MAPS: A Massively Parallel Processor with 3D Stacked Memory**  
National Security Agency, BAA-002-08  
Requested: \$900,000
2. **A Vertical Approach to 3D-Integrated High-Performance Processors**  
SRC Focus Center Research Projects, Center for Circuit and System Solutions (C2S2)  
Requested: \$600,000

**c. Not Funded**

1. **Fast and Reliable 3D Microarchitecture Design with Physical Planning**  
PIs: Sung Kyu Lim (ECE), Co-PI: Hsien-Hsin S. Lee (ECE)  
National Science Foundation  
Requested: \$573,647

**G. Research Proposals and Grants (Internal)**

None.

**H. Research Honors and Awards**

None.

### **III. SERVICE**

#### **A. Professional Activities**

##### **A.1 Membership and Activities in Professional Societies**

1. Member, Association for Computing Machinery (ACM)
2. Member, ACM SIG on Computer Architecture (SIGARCH)
3. Member, Institute of Electrical and Electronics Engineers (IEEE)
4. Member, IEEE Computer Society
5. Member, IEEE Technical Committee on Microarchitecture (TC-uARCH)

##### **A.2 Conference Committee Activities**

###### **a. Conferences**

1. Program Committee Member, International Symposium on High Performance Computer Architecture (HPCA), 2009.
2. Program Committee Member, IEEE International Conference on Computer Design (ICCD), 2009.
3. Program Committee Member, International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2009.
4. Program Committee Member, IEEE International Symposium on Performance Analysis of Software and Systems (ISPASS), 2008.
5. Program Committee Member, ACM International Conference on Computing Frontiers, 2008.
6. Program Committee Member, IEEE International Symposium on Microarchitecture (MICRO), 2007.
7. Program Committee Member, ACM International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES), 2007.
8. Program Committee Member, ACM International Conference on Computing Frontiers, 2007.
9. Program Committee Member, IEEE International Conference on Computer Design (ICCD), 2007.
10. Program Committee Member, ACM International Conference on Computing Frontiers, 2006.
11. Program Committee Member, IEEE International Conference on Computer Design (ICCD) 2006.

###### **b. Workshops**

1. Program Committee Member, 2nd Value Prediction Workshop, 2004, in conjunction with ASPLOS.
2. Program Committee Member, 2nd Workshop on Modeling, Benchmarking and Simulation, 2006/2008, in conjunction with ISCA.
3. Program Committee Member, 5th-7th Workshop on Duplicating, Deconstructing, and Debunking, 2006/2007/2008, in conjunction with ISCA.
4. Program Committee Member, 1st and 2nd Workshop on Architectural Support for Gigascale Integration, 2006/2007, in conjunction with ISCA.
5. Program Committee Member, 2nd Championship Branch Prediction Contest, 2006, in conjunction with MICRO 2006.

###### **c. Other**

1. Program Committee Member, IEEE Micro Special Issue on Top-Picks from Computer Architecture Conferences, 2008.

### **A.3 Workshops and External Courses**

1. Co-Organizer, Workshop on Duplicating, Deconstructing and Debunking (WDDD), in conjunction with ISCA 2008.
2. Co-Organizer, Tutorial on 3D Integration for (Micro)Architects, in conjunction with MICRO 2006, ISCA 2008.

### **B. On-campus Georgia Tech Committees**

1. PhD Admissions Committee, College of Computing. 2004-2005 Academic Year.
2. Technology Symposium Organizing Committee, 2005.
3. PhD Admissions Committee, College of Computing. 2005-2006 Academic Year.
4. PhD Teaching Assistant Requirements Committee, College of Computing. 2006-2007 Academic Year.
5. CoC/ECE Joint Program Committee, College of Computing. 2006-2007 Academic Year.
6. PhD Admissions Committee, College of Computing. 2007-2008 Academic Year.

### **C. Member of Ph.D. Examining Committees**

#### **Ph.D. Examining Committees – Georgia Tech**

**Chad Huneycutt**, College of Computing

Title: Optimizations for SoftCache Miss Latency Compensation

Advisor: Santosh Pande

**Weidong Shi**, College of Computing

Title: Effective and Efficient Architectural Support for Trusted Computing and Digital Rights Management

Advisor: Hsien-Hsin S. Lee

**Lakshmi Chakrapani**, College of Computing

Title: Probabilistic Architectures

Advisor: Krishna Palem

**Chenyu Yan**, College of Computing

Title: Hardware Support for Improving Security and Performance of Memory Sub-Systems

Advisor: Milos Prvulovic

**Guru Prasad Venkataramani**, College of Computing

Title: Low-cost and Efficient Architectural Support for Correctness and Performance Debugging

Advisor: Milos Prvulovic

#### **D. External Member of Ph.D. Examining Committees**

##### **Ph.D. Examining Committees – Georgia Tech**

**Martin Saint-Laurent**, School of Electrical and Computer Engineering, Fall 2004

Title: Modeling and Analysis of High-Frequency Microprocessor Clocking Networks

Advisor: Madhavan Swaminathan

**Peter Sassone**, School of Electrical and Computer Engineering, Spring 2005

Title: Characterization and Avoidance of Critical Pipeline Structures

Advisor: D. Scott Wills

**Mongkol Ekpanyapong**, School of Electrical and Computer Engineering, Fall 2005

Title: Microarchitecture-Aware Physical Planning for Deep Submicron Technology

Advisor: Sung Kyu Lim

**Jacob R. Minz**, School of Electrical and Computer Engineering, Summer 2006

Title: Physical Design Automation for System-on-Packages and 3D-Integrated Circuits

Advisor: Sung Kyu Lim

**Hongkyu Kim**, School of Electrical and Computer Engineering, Fall 2006

Title: Architectural Enhancements for Efficient Operand Transport in Multimedia Systems

Advisor: D. Scott Wills and Linda Wills

**Michael Healy**, School of Electrical and Computer Engineering

Title: Multi-Objective Microarchitectural Floorplanning for Single- and Many-Tier Systems

Advisor: Sung Kyu Lim

**Chinnakrishnan Ballapuram**, School of Electrical and Computer Engineering

Title: SOLAR: Semantics-Oriented Low Power Architecture

Advisor: Hsien-Hsin S. Lee

#### **E. External Member of Masters Examining Committees**

**Juno Baek**, Department of Electrical Engineering

Title: Modeling Current-Switching Noise Effects in a 3D Integrated Processor

Advisor: Hsien-Hsin S. Lee

**Michael Healy**, School of Electrical and Computer Engineering

Title: Performance and Temperature Aware Floorplanning Optimization for 2D and 3D Microarchitectures

Advisor: Sung Kyu Lim

#### **F. Research Project Reviewer**

1. National Science Foundation, CAREER (CCF/CPA) Award review panel, 2007.
2. National Science Foundation, CPA review panel, 2008.

## **IV. NATIONAL AND INTERNATIONAL PROFESSIONAL RECOGNITION**

### **A. Invited Conference Session Chairmanships**

1. 2nd Value Prediction Workshop, 2004.
2. Session on *Instruction Issue, Scheduling and Prediction*, at the International Conference on Computer Design (ICCD), 2005.
3. Session on *Power*, at the International Symposium on Performance Analysis of Systems and Software (ISPASS), 2006.
4. Session on *Superscalar Processors*, at the International Symposium on Microarchitecture (MICRO), 2006.
5. Session on *Cache Replacement Policies*, at the International Symposium on Microarchitecture (MICRO), 2007.

### **B. Invited Panel Speaker**

1. Third Workshop on Temperature-Aware Computer Systems, 2006, in conjunction with ISCA. Panel Speaker.

### **C. Editorial Boards for Technical Journals**

1. Editorial board member, Journal of Instruction Level Parallelism

### **D. Reviewer Work for Technical Journals and Publishers**

1. Reviewer for:

#### **Journals**

- ACM Transactions on Computer Systems
- ACM Transactions on Architecture and Compiler Optimization
- IEEE Transactions on Computers
- IEEE Transactions on VLSI
- IEEE Journal of Solid-State Circuits
- IEEE Computer Architecture Letters
- IEEE Micro (Magazine)
- IEE Computers and Digital Techniques
- Journal of Instruction Level Parallelism

#### **Conferences** (sorted alphabetically by conference acronym)

- ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2006
- IEEE International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES) 2005, 2007
- ACM International Conference on Computing Frontiers (CF) 2006-2008
- IEEE International Symposium on Code Generation and Optimization (CGO) 2006
- European Conference on Parallel Processing (Euro-Par) 2005
- IEEE High Performance Computer Architecture (HPCA) 2005-2008
- IEEE International Conference on Computer Design (ICCD) 2005-2007
- IEEE International Conference on Parallel and Distributed Systems (ICPADS) 2004
- IEEE International Symposium on Computer Architecture (ISCA) 2006-2008
- IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2004, 2006
- IEEE International Symposium on Microarchitecture (MICRO) 2004-2007
- ACM/IEEE International Symposium on Parallel Architectures and Compilation Techniques (PACT) 2005
- IEEE International System-on-Chip Conference (SOCC) 2005

## **E. Other Conference Service Positions**

1. ACM ISCA vs. STOC 2007 Ice Hockey game co-organizer
2. ACM ISCA 2006 Ice Hockey game organizer
3. IEEE ISPASS 2007 Publicity Chair
4. ACM ISCA 2009 Publications Chair

## **V. OTHER CONTRIBUTIONS**

### **A. Seminar Presentations**

1. Branch Prediction Fusion. University of Washington, Seattle, WA; May 2003. Invited.
2. High-Performance 3D Microarchitecture Design. IBM Corporation, Austin, TX; February 2006. Invited.
3. High-Performance 3D Microarchitecture Design. AMD Corporation, Austin, TX; February 2006. Invited.
4. High-Performance 3D Microarchitecture Design. Interconnect Focus Center, Atlanta, GA; March 2006. Invited.
5. 3D Integration: The Next Revolution in the Design of Microprocessors. Korea University, Seoul, South Korea; April 2007. Invited.
6. 3D Integration: The Next Revolution in the Design of Microprocessors. Samsung Corporation, Yongin-City, South Korea; April 2007. Invited.
7. 3D Integration: The Next (R)Evolution in the Design of Microprocessors. North Carolina State University, Raleigh, NC; September 2007. Invited.
8. 3D Integration: The Next (R)Evolution in the Design of Microprocessors. Northwestern University, Chicago, IL; October 2007. Invited.
9. 3D Integration: The Next (R)Evolution in the Design of Microprocessors. IBM T. J. Watson Research Center, Yorktown Heights, NY; March 2008. Invited.
10. 3D Integration: The Next (R)Evolution in the Design of Microprocessors. University of Texas at Austin; September 2008. Invited.