

CS 6290 Homework 1

Fall 2007

Due: 9/11 at start of class

There are four problems in this homework. Each problem is worth 5 points. You should turn in your solutions one problem per page, in-order (problem 1 first, then problem 2, etc.). Show your work. No points will be given for providing only a numeric answer without showing or explaining (briefly, please) how you got the answer.

Problem 1:

A processor has a clock frequency of 5GHz and is running a program that executes 5 billion instructions from start to finish. The instruction mix of this program is 20% branches, 20% loads, 10% stores, and 50% ALU. The average IPC is 1 for branches, 0.5 for loads, 1 for stores, and 2 for ALU instructions. What is the total execution time for this program on this processor?

Problem 2:

You are considering two possible enhancements for the processor described in Problem 1. One enhancement is a better memory organization, which would improve the average IPC for load instructions from 0.5 to 1. The other enhancement is a new multiply-and-add instruction that would reduce the number of ALU instructions by 20% while still maintaining the average IPC of 2 for the remaining ALU instructions. Unfortunately, there is room on the processor chip for only one of these two enhancements, so you must choose the enhancement that provides better overall performance. Which one would you choose?

Problem 3:

You are developing the DWARF II, a new processor based on the MINE instruction set architecture. This ISA is very similar to the MIPS ISA, but has only four registers: lamp, pick, shovel, and dirt. The DWARF microarchitecture has seven additional physical registers: dopey, grumpy, doc, happy, bashful, sneezy, and sleepy. The processor is executing the following sequence of instructions (see other page):

```
ADD pick, shovel, dirt
NOT lamp, shovel
ADD dirt, pick, dirt
SUB dirt, dirt, lamp
MUL pick, lamp, dirt
AND shovel, lamp, dirt
XOR lamp, pick, dirt
BNE lamp, pick, Label
```

Note: This is a 3-address ISA where destination register is listed first. In other words, SUB X,Y,Z means $X=Y-Z$

- a) What is the available ILP for this code?
- b) Assuming all renaming gets done before any instruction commits, show the instruction sequence after register renaming. Before the renaming begins, all seven physical registers are in the free list and their order in the free list is: dopey, grumpy, doc, happy, bashful, sneezy, and (finally) sleepy.
- c) What is the available ILP after renaming?

Problem 4:

Using Tomasulo's algorithm, for each instruction in the following sequence determine when (in which cycle, counting from the start) it issues, begins execution, and writes its result to the CDB. Assume that the result of an instruction can be written in the last cycle of its execution. The execution time of all instructions is two cycles, except for multiplication (which takes 4 cycles) and division (which takes 8 cycles). The processor has one multiply/divide unit and one add/subtract unit. The multiply/divide unit has two reservation stations and the add/subtract unit has four reservation stations. None of the execution units is pipelined – each can only be executing one instruction at a time. If a conflict for use of the CBD occurs, the result of the add/subtract unit has priority over the result of the multiply/divide unit. Assume that at start all instructions are already in the instruction queue, but none has yet been issued to any reservation stations. The processor can issue only one instruction per cycle, and there is only one CDB for writing results.

```
DIV F4, F5, F6
ADD F1, F2, F4
ADD F2, F5, F3
SUB F4, F4, F2
ADD F3, F1, F2
MUL F1, F2, F3
ADD F3, F3, F3
SUB F5, F4, F1
ADD F5, F6, F3
```