

CS6290 Homework 1
Fall 2007
Solutions

Problem 1:

Instruction Type	Freq. of Inst.	CPI
Branches	20%	1
Loads	20%	2
Stores	10%	1
ALU	50%	0.5

$$\text{Total Execution Time} = \frac{(0.2 * 1 + 0.2 * 2 + 0.1 * 1 + 0.5 * 0.5) \text{ cycles/inst} \times 5B \text{ inst}}{5G \text{ cycles/sec}}$$

= 0.95 seconds

Problem 2:

a) Better memory organization: CPI for loads reduced to 1.

$$\text{CPU Time} = (0.2 * 1 + 0.2 * 1 + 0.1 * 1 + 0.5 * 0.5) * 5B / 5G = 0.75 \text{ seconds}$$

b) Reduced the number of ALU instructions: # of ALU instructions: $5B * 50\% * 80\%$.

$$\text{CPU Time} = (0.2 * 1 + 0.2 * 2 + 0.1 * 1 + 0.5 * 0.8 * 0.5) * 5B / 5G = 0.90 \text{ seconds}$$

Therefore, better memory organization gives better performance.

Problem 3:

a) ILP before register renaming: $ILP = \# \text{ of instructions} / \text{Longest Path in Dep' Graph} = 8/6$

cycle 1: I1, I2

cycle 2: I3

cycle 3: I4

cycle 4: I5, I6

cycle 5: I7

cycle 6: I8

Please note that the last instruction is BNE, a branch instruction which never writes (except for condition flags).

b) After register renaming: ILP remains the same = $8/6$

```
ADD dopey, shovel, dirt
```

```
NOT grumpy, shovel
```

```
ADD doc, dopey, dirt
```

```
SUB happy, doc, grumpy
```

```
MUL bashful, grumpy, happy
```

```
AND sneezy, grumpy, happy
```

```
XOR sleepy, bashful, happy
```

```
BNE sleepy, bashful, label
```

Note that every destination registers need to be renamed.

Problem 4:

	Instructions	IS	EX	W	Note
1	DIV F4, F5, F6	1	2	9	
2	ADD F1, F2, F4	2	10	11	Wait for F4
3	ADD F2, F5, F3	3	4	5	
4	SUB F4, F4, F2	4	12	13	Waits for F4
5	ADD F3, F1, F2	5	14	15	Waits for F1, Adder full
6	MUL F1, F2, F3	6	16	20	Waits for F3, CDB conflict
7	ADD F3, F3, F3	7	16	17	Waits for F3
8	SUB F5, F4, F1	12	21	22	Reservation full, Waits for F1
9	ADD F5, F6, F3	14	18	19	Reservation full, Waits for F3

The problem clearly assumed that the result of an instruction can be written in the last cycle of its execution. Some of students ignored this assumption, so made a mistake: for example, the first instruction writes at cycle 10.