

**SAMANTIKA SUBRAMANIAM**  
**2401 Windy Hill Road, Apt 1851M**  
**Marietta, GA 30067**  
**404 934 4902**  
[samantik@cc.gatech.edu](mailto:samantik@cc.gatech.edu),  
[www.cc.gatech.edu/~samantik](http://www.cc.gatech.edu/~samantik)

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My research interest is in high performance computer architecture. I am particularly interested in the impact of long-latency memory instructions on the efficiency of current and future processors. As the initial part of my research I explored the dependencies between memory instructions to design faster processors and reduce the design complexity of traditional structures that support out-of-order memory scheduling. Since then I have focused my attention on allied applications of memory dependence prediction. I first designed a new, high-performing instruction fetch policy for SMT machines which is cognizant of memory latencies and am currently exploring the impact of critical memory instructions on the performance of the processor as well as their application in resource management.

### Education

- PhD Computer Science, Georgia Institute of Technology, Fall 2006 – present
- Minor in Finance, Georgia Institute of Technology, May 2007, GPA: 4.0
- MS Computer Science, Georgia Institute of Technology, December 2006, GPA: 4.0
- B.E. Computer Engineering, Mumbai University, India. May 2004  
Percentage: 75% Equivalent GPA: 3.8

### Publications

- **Refereed Conferences**

- Samantika Subramaniam, Gabriel H. Loh, “Store Vectors for Scalable Memory Dependence Prediction and Scheduling”, in the International Symposium on High-Performance Computer Architecture (HPCA), February 2006.

- **Best Student Presentation Award**

- Samantika Subramaniam, Gabriel H. Loh, “Fire-and-Forget: Load/Store Scheduling with No Store Queue at All”, in the International Symposium on Microarchitecture (MICRO), December 2006.

- **Best Student Presentation Award**

- Samantika Subramaniam, Milos Prvulovic, Gabriel H. Loh, “PEEP: Exploiting Predictability of Memory Dependences in SMT Processors”, in the International Symposium on High-Performance Computer Architecture (HPCA), February 2008.

- **Refereed Journals**

- Samantika Subramaniam and Gabriel H. Loh, “Design and Optimization of the Store Vectors Memory Dependence Predictor”, to appear in the ACM Transactions on Architecture and Code Optimization (Accepted with revisions).

- **Refereed Workshops**

- Rahul V. Garde, Samantika Subramaniam and Gabriel H. Loh, “Deconstructing the Inefficacy of Global Cache Replacement Policies”, to appear in the 7th Workshop on Duplicating, Deconstructing, and Debunking (WDDD) 2008 (held in conjunction with ISCA 2008).

- **Selected Poster**

- Samantika Subramaniam and Gabriel H. Loh, “Exploiting Predictability of Memory Dependences to mitigate load latencies”, in the Grace Hopper Celebration for Women in Computing Conference (GHC), October 2007.

### Work Experience

- Graduate Research Intern at Intel Corporation- MRL, Santa Clara (June 2007-December 2007)  
Researched various fetch policies in SMT machines and developed a new fetch policy to assist efficient thread switching.  
Designed and implemented a critical load instruction identifier unit and researched its applications in resource management in OOO cores. (**Invention disclosure filed**)
- Graduate Research Assistant for Dr. Gabriel Loh (2005-present)  
Research focus included optimizing SMT fetch policies, alternate scalable designs for traditional load-store queues and the design and implementation of a high performance and scalable memory dependence predictor.
- Graduate Research Assistant with School of Civil Engineering, Georgia Tech (Fall 2004)

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Responsibilities included designing an application in Visual Basic and Microsoft Access to manage software licensing.

- Researched with Prof. Brian Cooper in developing a database interface to the 'deep web' using XML middleware. (Fall 2004)

#### **Honors and Awards**

- Outstanding Graduate Research Assistant Award 2008 awarded by College of Computing, Georgia Tech.
- Intel Fellowship 2008-2009.
- Winner, Best Student Presentation, HPCA 2006.
- Winner, Best Student Presentation, MICRO 2006.

#### **Academic Projects**

- Implemented a fetch policy for an SMT processor based on memory dependence prediction.
- Designed a "Speculative Stores in Cache" mechanism inspired by the Transmeta Efficeon to provide a way for store instructions to write to cache as early as possible.
- Designed and worked with a team in a project titled "Dynamic resource monitoring". Project involved using cluster parameters like load balancing, client-server workload etc. to efficiently distribute work.
- Other graduate level projects include exploring efficient client-server environments and implementation and analysis of some influential work in Computer Microarchitecture.

#### **Skills**

- Tools: SimpleScalar, CACTI
- Languages: C, C++, Perl, Prolog, Matlab

#### **Service and Affiliations**

- Reviewer for CASES 2008, MICRO 2008
- IEEE student member (2001-2005)
- ACM student member (2005- Present)

#### **Personal**

- Citizenship: India
- Visa Status: F1

#### **References**

- Prof Gabriel H. Loh  
Assistant Professor,  
School of Computer Science,  
Georgia Institute of Technology  
Atlanta GA 30332.
- Dr. Hong Wang  
Senior Principal Engineer,  
Director,  
Microarchitecture Research Lab,  
Intel Corporation,  
Santa Clara CA 95054.
- Prof Milos Prvulovic  
Assistant Professor,  
School of Computer Science,  
Georgia Institute of Technology  
Atlanta GA 30332.