

Vishal Gupta

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AREAS OF INTEREST

Operating System, Virtualization, and Distributed Systems
Research Focus: Energy-Efficient Resource Management on Heterogeneous Platforms

EDUCATION

Georgia Institute of Technology, Atlanta, GA

Ph.D., Computer Science, Advisor: Dr. Karsten Schwan (GPA:4.0/4.0) Expected 2013

University of North Carolina at Chapel Hill, NC

M.S., Computer Science (GPA:N/A) 2006-2008

Indian Institute of Technology (IIT) Madras, India

B.Tech., Computer Science & Engineering (GPA:8.59/10) 2002-2006

WORK EXPERIENCE

- **Intel Labs**, Hillsboro, OR (Internship) June 2011-Jan 2012
Worked with the System Architecture Labs on techniques to extend the dynamic power range of client devices using heterogeneous multicore processors. Specifically, this work uses a mix of heterogeneous cores to provide both high-performance and low-power modes while maintaining energy-efficiency.
- **Microsoft Research**, Redmond, WA (Internship) May-July 2010
Performed an opportunity analysis of heterogeneous chip multiprocessors for the datacenter applications. Using analytical models, this work presents an analysis of achievable energy savings of heterogeneous multicore processors over homogeneous processors for area equivalent configurations.
- **Google**, Mountain View, CA (Internship) Jun-Aug 2009
Worked on non-temporal cache prefetching techniques to prevent CPU cache pollution. Using reuse distance as an input, this work modifies an application binary to insert non-temporal access prefetch instructions at appropriate positions to not cache data with no temporal locality.
- **IBM India Research Laboratory (IRL)**, New Delhi, India (Internship) June-July 2008
Worked on parallelizing a sequential SAT solver named Minisat on Blue-Gene. It was designed to be scalable using a state machine based coordination mechanism and a master-slave architecture.
- **Yahoo!**, Sunnyvale, CA (Internship) May-Aug 2007
Developed an API which enables users to categorize data by applying keyword tags and perform a search using these tags. Also, implemented a simple web-based front-end to use this API.
- **Open-Silicon**, Bangalore, India (Internship) May-Jul 2005
Performed standard cell library characterization for digital gates, latches, and flip-flops using Spice.
- **RISE Lab**, Dept. of CSE, IIT Madras, India (Internship: sponsored by Intel India) June-Aug 2004
Testing of decoder unit for a behavioral model simulator of Intel x86 core.

TEACHING EXPERIENCE

- **Distributed Computing**: Teaching assistant at Georgia Tech 2009
- **Computer & Network Security**: Teaching assistant at UNC Chapel Hill 2008
- **Digital Logic Design**: Teaching assistant at UNC Chapel Hill 2007

RESEARCH PUBLICATIONS

- Vishal Gupta, Paul Brett, David Koufaty, Dheeraj Reddy, Scott Hahn, Karsten Schwan, and Ganapati Srinivasa. HeteroMates: Providing high dynamic power range on client devices using heterogeneous core pairing. In *IEEE International Green Computing Conference, (IGCC)*, 2012. (To appear).
- Vishal Gupta, Paul Brett, David Koufaty, Dheeraj Reddy, Scott Hahn, Karsten Schwan, and Ganapati Srinivasa. The forgotten ‘Uncore’: On the energy-efficiency of heterogeneous cores (Short Paper). In *USENIX annual technical conference, (ATC)*, 2012. (To appear).
- Vishal Gupta, Ripal Nathuji, and Karsten Schwan. An analysis of power reduction in datacenters using heterogeneous chip multiprocessors. In *ACM SIGMETRICS Perform. Eval. Rev. (PER)*, Dec. 2011. (Invited paper)
- Vishal Gupta, Paul Brett, Scott Hahn, David Koufaty, Mishali Naik, Paolo Narvaez, Abirami Prabhakaran, Dheeraj Reddy, Karsten Schwan, and Ganapati Srinivasa. Extending the dynamic power range of client devices using heterogeneous multicore processors. In *Proceedings of the Workshop on SoCs, Heterogeneous Architectures and Workloads, SHAW-3*, New Orleans, LA, USA, Feb 2012.
- Vishal Gupta, Ripal Nathuji, and Karsten Schwan. An analysis of power reduction in datacenters using heterogeneous chip multiprocessors. In *Proceedings of the ACM SIGMETRICS GreenMetrics’11 Workshop*, San Jose, CA, USA, June 2011.
- Vishal Gupta and Ripal Nathuji. Analyzing performance asymmetric multicore processors for latency sensitive datacenter applications. In *Proceedings of the Workshop on Power aware computing and systems, (HotPower’10)*, Vancouver, BC, Canada, October 2010.
- Gennette Gill, Vishal Gupta, and Montek Singh. Performance estimation and slack matching for pipelined asynchronous architectures with choice. In *Proceedings of the 2008 IEEE/ACM International Conference on Computer-Aided Design, ICCAD ’08*, Piscataway, NJ, USA, 2008.
- Gennette Gill, Vishal Gupta, and Montek Singh. Robust Performance estimation and slack matching for pipelined asynchronous architectures with choice. In *Proceedings of the ACM/IEEE International Workshop on Logic and Synthesis, IWLS ’08*, Lake Tahoe, CA, USA, June 2008.
- K. Najeeb, Vishal Gupta, V. Kamakoti, and Madhu Mutyam. Temporal redundancy based encoding technique for peak power and delay reduction of on-chip buses. *J. Low Power Electronics*, 2(3):425–436, December 2006.
- K. Najeeb, Vishal Gupta, and V. Kamakoti. Delay and peak power minimization for on-chip buses using temporal redundancy. In *Proceedings of the 16th ACM Great Lakes symposium on VLSI, GLSVLSI ’06*, New York, NY, USA, 2006. ACM.

RESEARCH SUMMARY

- **Energy-Efficient Operation on Client Devices and Server Systems using Heterogeneous Multicore Platforms (CERCS Systems Research Group, Georgia Tech):** Currently working with Dr. Karsten Schwan on resource management techniques to support novel architectural solutions involving heterogeneous multicores consisting of cores with different performance and power characteristics, with the aim of maximizing energy-efficiency for large-scale datacenters and handheld mobile devices.
- **Energy Conservation in Asynchronous Systems Using Self-Adaptive Fine-Grain Voltage Scaling (M.S. Thesis, UNC Chapel Hill):** Proposed a new voltage scaling technique for asynchronous systems which allows fine-grain scaling of supply voltage, i.e. each stage in the pipeline is allowed to scale its voltage independently which gives higher energy savings as compared to coarse grain techniques.
- **Delay and Power Minimization in On-Chip Buses using Temporal Redundancy (B.Tech. Thesis, IIT Madras):** Proposed two novel bus encoding schemes to minimize delay and power consumption in on-chip buses. Unlike the previous techniques which used spatial redundancy (extra lines) for encoding, our technique uses temporal redundancy (multiple transmissions) for reducing crosstalk effects.

ACADEMIC AWARDS

- USENIX Student Grant for OSDI Conference, Vancouver, BC, Canada 2010
- Winner of Yahoo! Hack Event for Upcoming HotJobs application. 2007
- IEEE Asian Test Symposium (ATS) fellowship, Kolkata, India. 2005
- CSIR fellowship from Central Electronic Engineering Research Institute (CEERI), Pilani, India. 2000
- Merit scholarship from Govt. of India for achieving 12th rank in 10th grade examination. 2000

COMPUTER SKILLS

Platforms: Linux, Xen, x86

Programming: C, C++, Java, Verilog, Python

Tools & APIs: MPI, openMP, GDB, Git, Latex, Matlab

PROFESSIONAL SERVICES

- Member of Graduate Travel Committee for managing conference travel funds. 2011-2012
- Administrator of CERCS Lab, Georgia Tech for managing computing resources. 2009-2011
- Secretary of IITM CS Club responsible for arranging various extra-curricular activities. 2005-2006

COURSE WORK

- **Graduate:** Operating Systems, Computer Architecture, Distributed Computing, Algorithm Analysis, Computer Networks, High Performance Computing
- **Minor:** Principles of Management, Management of Technology, E-Commerce
- **Undergraduate:** Compilers, Database Systems, Software Engineering, Real Time Systems, Artificial Intelligence, Computer Graphics, Graph Theory, Probability & Statistics, Operations Research

PROJECT SUMMARY

- **Operating System Kernel:** Developed a thin-kernel for a distributed operating system which supports process management, local and distributed interprocess communication, process synchronization, and distributed terminal devices for I/O. Finally, a teleconferencing console was built using this kernel.
- **Superscalar Multi-processor System:** Participated in a 3-member team which developed a superscalar multiprocessor system with MESI protocol for cache coherency and Tomasulo protocol for instruction level parallelism in Verilog HDL and burnt in on FPGA.
- **MapReduce using MPI:** Developed a simplified implementation of Google MapReduce API using MPI. Fault-tolerance was not implemented as part of this implementation.
- **File System:** Implemented a simple file system in Java which could read and write blocks of data to main memory module by issuing I/O system calls to an operating system model which simulated disk behavior. Also, buffer cache system was implemented.
- **Pascal Compiler:** Implemented a simple working compiler front end for the Pascal language in C which converts source program to x86 assembly code which can be assembled using Nasm.

REFERENCES

- Dr. Karsten Schwan, Regents' Professor, College of Computing, Georgia Tech, Atlanta, GA
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- Dr. Scott Hahn, Principal Engineer, Intel Labs, Hillsboro, OR
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- Ganapati Srinivasa, Principal Engineer, Intel Corporation, Hillsboro, OR
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