Hyesoon Kim

hyesoon@cc.gatech.edu
Assistant Professor
School of Computer Science
Georgia Institute of Technology
`http://www.cc.gatech.edu/~hyesoon`

Research Interests

- Compiler and hardware support for heterogeneous (GPU/CPU) architectures.
- Computer architecture, compiler-microarchitecture interaction.
- Low-power high-performance embedded processors, especially for automotive systems.
- Compiler and hardware support for dynamic optimizations, virtual machines, and binary instrumentation.

Education

Ph.D. in Electrical and Computer Engineering, August 2007
The University of Texas at Austin
Advisor: Professor Yale N. Patt

MSE in Electrical and Computer Engineering, May 2003
The University of Texas at Austin

MS in Mechanical Engineering, Feb. 1998
Seoul National University, South Korea

BS in Mechanical Engineering, Feb. 1996
Korea Advanced Institute of Science and Technology (KAIST), South Korea

Awards

- One paper (of eleven) selected for IEEE Micro's "Top Picks in Computer Architecture Conferences," 2006.
  Diverge-Merge Processor (DMP): Generalized and Energy-Efficient Dynamic Predication
- Two papers (of thirteen) selected for IEEE Micro's "Top Picks in Computer Architecture Conferences," 2005.
  Wish Branches: Enabling Adaptive and Aggressive Predicated Execution
  Efficient Runahead Execution: Power-efficient Memory Latency Tolerance

Research Experience

The University of Texas at Austin, Electrical and Computer Engineering, *Jun. 2001 - Jun. 2007*
Research Assistant for Prof. Yale N. Patt

- Dissertation: *Adaptive Predication via Compiler-Microarchitecture Cooperation*.
- Main research results:
  - Adaptive and energy-efficient predication via compiler/hardware cooperation:
    - Dynamic predication [MICRO 2006][IEEE-MICRO TOP PICKS 2007].
    - Wish branches [MICRO 2005][IEEE-MICRO TOP PICKS 2006].
    - Compiler algorithms to generate predicated code for high-performance processors [CGO 2007].
  - Efficient profiling techniques to predict input-set dependency of program behavior: 2D-profiling [CGO 2006].
  - Efficient memory latency tolerance techniques:
    - Runahead execution [ISCA 2005] [MICRO 2005] [IEEE-MICRO TOP PICKS 2006] [IEEE-TC 2006] [IEEE-CAL 2005].
    - Bandwidth-efficient data prefetching [HPCA 2007].
  - Wrong-path execution to improve processor performance and efficiency:
    - Wrong-path events [MICRO 2004].
    - Wrong-path memory effects [WMPI 2004][IEEE-TC 2005][SBAC-PAD 2004][IJPP 2005].
  - Power-efficient processors: limited out-of-order execution processors, performance-aware pipeline gating [HPCA 2008].
  - Hardware support to improve the performance of managed and object oriented languages and virtual machines:
    - Efficient indirect branch prediction [ISCA 2007], program phase detection and analysis.
    - Efficient indirect branch predication [IEEE-CAL 2007][ASPLOS 2008]

Seoul National University, Mechanical Engineering, *Jan. 1996 - Oct. 1998*
Research Assistant for Prof. S. Ken Kauh

- Developed Engine Control Unit (ECU) and Air/Fuel ratio control logic (1996-1998).
- Designed individual cylinder A/F control logic, funded by Samsung Motor Company (1997-1998).
- Implemented ECU hardware for feedback mixer, funded by Kia Motor Company (1996).

Industry Experience

Intel Corporation, VSSAD - Hudson, MA, USA, Supervisor: Dr. Robert Cohn
Graduate Technical Intern, *Jun. 2006 – Sep. 2006*

- Researched hardware support to improve the performance of managed and object-oriented languages.
- Developed a novel and cost-effective way of handling indirect branch instructions.
- Implemented the 2D-profiling algorithm [CGO 2006] into Intel's commercial compiler (ICC).
- Studied novel predicated code generation algorithms using branch misprediction profile information.
- Analyzed performance in Itanium and x86 processors using hardware performance counters.

Intel Corporation, Microprocessor Research Labs - Hillsboro, OR, USA, Supervisor: Dr. Jared Stark
Graduate Technical Intern, *May 2004 – Aug. 2004*

- Researched new register renaming algorithms and front-end designs to reduce dynamic/static power in a low-power processor.
- Designed hardware prefetching algorithms to reduce the memory bandwidth requirements in a high performance processor.

Intel Corporation, Microprocessor Research Labs - Hillsboro, OR, USA, Supervisor: Dr. Jared Stark
Graduate Technical Intern, *May 2003 – Aug. 2003*

- Developed an IA-64 microarchitecture simulator.
- Studied predicated execution to reduce the branch misprediction penalty.
- Investigated hardware techniques to improve predicated execution.

Intel Corporation, Desktop Platforms Group - Hillsboro, OR, USA, Supervisor: Eric Sprangle
Graduate Technical Intern, *May 2002 – Aug. 2002*

- Studied novel prefetching algorithms to tolerate the memory latency of a next-generation IA-32 processor.
- Designed a new program phase detection algorithm that provides architectural support for a dynamic optimization system.

Hyundai Motor Company, Research Center - South Korea
Researcher, *Jul. 1999 – Jul. 2000*
Visiting Researcher, *Mar. 1998 – Jun. 1999*

- Developed engine control logic designs and experimented with emission control techniques (1998).
- Researched an electro-mechanical valve (EMV) engine (1999 - 2000).

Refereed Conference Publications

1. José A. Joao, Onur Mutlu, Hyesoon Kim, Rishi Agarwal, and Yale N. Patt, "Improving the Performance of Object-Oriented Languages with Dynamic Predication of Indirect Jumps," to appear in *Proceedings of the 13th International Conference on Architectural Support for Programming Languages and Operating Systems (***ASPLOS-13)**, Seattle, WA, March 2008..
2. Chang Joo Lee, Hyesoon Kim, Onur Mutlu, and Yale N. Patt, "Performance-Aware Speculation Control Using Wrong Path Usefulness Prediction," to appear in *Proceedings of the 14th International Symposium on High-Performance Computer Architecture (***HPCA-14***)*, Salt Lake City, UT, February 2008.
3. Hyesoon Kim, José A. Joao, Onur Mutlu, Chang Joo Lee, Yale N. Patt, Robert S. Cohn, "VPC Prediction: Reducing the Cost of Indirect Branches via Hardware-Based Dynamic Devirtualization," *the 34th Annual International Symposium on Computer Architecture* **(ISCA-34)**, San Diego, CA, June 2007.
4. Hyesoon Kim, José A. Joao, Onur Mutlu, Yale N. Patt, "Profile-assisted Compiler Support for Dynamic Predication in Diverge-Merge Processors ," *Proceedings of the 5th International Symposium on Code Generation and Optimization (***CGO-5***)*, San Jose, CA, March 2007.
5. Santhosh Srinath, Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Feedback Directed Prefetching: Improving the Performance and Bandwidth-Efficiency of Hardware Prefetchers ," *Proceedings of the 13th International Symposium on High-Performance Computer Architecture (***HPCA-13***)*, Phoenix, AZ, February 2007. **Nominated for the Best Paper Award by the Program Committee.**

6. Hyesoon Kim, José A. Joao, Onur Mutlu, Yale N. Patt, "Diverge-Merge Processor (DMP): Dynamic Predicated Execution of Complex Control-Flow Graphs Based on Frequently Executed Paths ," *Proceedings of the 39th Annual International Symposium on Microarchitecture (***MICRO-39***)*, Orlando, FL, December 2006. **One of the 11 computer architecture papers of 2006 selected as Top Picks by IEEE Micro. Nominated for the Best Paper Award by the Program Committee.**
7. Hyesoon Kim, M. Aater Suleman, Onur Mutlu, Yale N. Patt, "2D–Profiling: Detecting Input-Dependent Branches with a Single Input Data Set," *Proceedings of the 4th International Symposium on Code Generation and Optimization (***CGO-4***)*, New York, NY, March 2006.
8. Hyesoon Kim, Onur Mutlu, Jared Stark, Yale N. Patt, "Wish Branches: Combining Conditional Branching and Predication for Adaptive Predicated Execution," *Proceedings of the 38th Annual International Symposium on Microarchitecture (***MICRO-38***)*, Barcelona, Spain, November 2005. **One of the 13 computer architecture papers of 2005 selected as Top Picks by IEEE Micro.**
9. Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Address-Value Delta (AVD) Prediction: Increasing the Effectiveness of Runahead Execution by Exploiting Regular Memory Allocating Patterns," *Proceedings of the 38th Annual International Symposium on Microarchitecture (***MICRO-38***)*, Barcelona, Spain, November 2005. **One of the five papers nominated for the Best Paper Award by the Program Committee.**
10. Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Techniques for Efficient Processing in Runahead Execution Engines," *Proceedings of the 32nd Annual International Symposium on Computer Architecture (***ISCA-32***)*, Madison, WI, USA, June 2005. **One of the 13 computer architecture papers of 2005 selected as Top Picks by IEEE Micro.**
11. David N. Armstrong, Hyesoon Kim, Onur Mutlu, Yale N. Patt, "Wrong Path Events: Exploiting Unusual and Illegal Program Behavior for Early Misprediction Detection and Recovery," *Proceedings of the 37th Annual International Symposium on Microarchitecture (***MICRO-37***)*, Portland, OR, USA, December 2004.
12. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, "Cache Filtering Techniques to Reduce the Negative Impact of Useless Speculative Memory References on Processor Performance," *Proceedings of the 16th IEEE International Symposium on Computer Architecture and High Performance Computing*, Foz do Iguacu, Brazil, October 2004.

Refereed Journal Publications

13. José A. Joao, Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Dynamic Predication of Indirect Jumps," **IEEE Computer Architecture Letters (CAL)**, vol. 6, May 2007
14. Hyesoon Kim, José A. Joao, Onur Mutlu, Yale N. Patt, "Diverge-Merge Processor (DMP): Generalized and Energy-Efficient Dynamic Predication," **IEEE Micro, Special Issue: Micro's Top Picks from Microarchitecture Conferences (MICRO TOP PICKS),** January/February 2007.
15. Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Address-Value Delta (AVD) Prediction: A Hardware Technique for Efficiently Parallelizing Dependent Cache Misses," ***IEEE Transactions on Computers (TC)***, Vol. 55, No. 12, pages 1491-1508, December 2006.
16. Hyesoon Kim, Onur Mutlu, Jared Stark, Yale N. Patt, "Wish Branches: Enabling Adaptive and Aggressive Predicated Execution," **IEEE Micro, Special Issue: Micro's Top Picks from Microarchitecture Conferences (MICRO TOP PICKS),** January/February 2006.
17. Onur Mutlu, Hyesoon Kim, Yale N. Patt, "Efficient Runahead Execution: Power-efficient Memory Latency Tolerance," **IEEE Micro, Special Issue: Micro's Top Picks from Microarchitecture Conferences (MICRO TOP PICKS)**, January/February 2006.
18. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, "An Analysis of the Performance Impact of Wrong-Path Memory References on Out-of-Order and Runahead Execution Processors," **IEEE Transactions on Computers (TC)**, Vol. 54, No. 12, pages 1556-1571, December 2005.
19. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, "Using the First-Level Caches as Filters to Reduce the Pollution Caused by Speculative Memory References," **International Journal of Parallel Programming (IJPP)**, Vol. 33, No. 5, pages 529-559, October 2005.
20. Onur Mutlu, Hyesoon Kim, Jared Stark, Yale N. Patt, "On Reusing the Results of Pre-Executed Instructions in a Runahead Execution Processor," **IEEE Computer Architecture Letters (CAL)**, vol. 4, January 2005.

Refereed Workshop Publication

21. Onur Mutlu, Hyesoon Kim, David N. Armstrong, Yale N. Patt, "Understanding the Effects of Wrong-Path Memory References on Processor Performance," *Proceedings of the 3rd ACM Workshop on Memory Performance Issues (WMPI), in conjunction with the 31st International Symposium on Computer Architecture*, Munchen, Germany, June 2004.

Patents

1. M. Choi, Hyesoon Kim, "Method for Detecting Malfunction of Car Cylinder" (US 6,273,075), August 2001.
2. M. Choi, Hyesoon Kim, "Method for Judging Failed Cylinder of a Vehicle" (KP 10-0305784-0000), August 2001.
3. Hyesoon Kim, "A Valve Timing Setting Method for Decreasing the Emission of Electro Mechanical Valve Engine" (KP 10-0354012-0000), September 2002.

Professional Activities

Program Committee member
International Symposium on Workload Characterization (IISWC), 2008

Reviewer
IEEE Transactions on Computers (TC), 2007
IEEE Computer Architecture Letters (CAL), 2006
International Symposium on Computer Architecture (ISCA), 2004, 2005, 2006, 2008
International Symposium on Microarchitecture (MICRO), 2004, 2005, 2006, 2007
International Conference on High Performance Computer Architecture (HPCA), 2003, 2005, 2006, 2007, 2008
International Conference on Supercomputing (ICS), 2002, 2003, 2005, 2007
International Conference on Parallel Architectures and Compilation Techniques (PACT), 2004
International Conference on High Performance Embedded Architectures And Compilers (HiPEAC), 2005, 2006
International Parallel and Distributed Processing Symposium (IPDPS), 2005, 2006
International Symposium on Workload Characterization (IISWC), 2006
International Conference on Computing Frontiers (CF), 2006, 2007
International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), 2004
Symposium of Integrated Circuits and Systems Design (SBCCI), 2005, 2006
Workshop on Application Specific Processors (WASP), 2003

Professional Memberships

Student member of IEEE and IEEE-CS, since 2005
Student member ACM and ACM-SIGARCH, since 2005