Hadi Esmaeilzadeh **January 2014**

Contact Information

Georgia Institute of Technology
College of Computing
266 Ferst Drive, KACB 2336
Atlanta, GA 30332-0765

http://www.cc.gatech.edu/~hadi/
hadi@cc.gatech.edu
Phone: (404) 385-1731
Office: KACB 2336

Research Interests

Computer architecture, novel computing and memory technologies, programming languages, mixed-signal VLSI circuits and systems, machine learning.

Employment

- **Assistant Professor.** School of Computer Science, Georgia Institute of Technology — Aug. 2013

Education

- **Ph.D. in Computer Science.** University of Washington — Aug. 2013
  Advisors: Doug Burger and Luis Ceze
  Dissertation: *Approximate Acceleration for a Post Multicore Era*
- **M.S. in Computer Science.** The University of Texas at Austin — Aug. 2010
  Advisors: Doug Burger and Kathryn McKinley
- **M.S. in Electrical and Computer Engineering.** University of Tehran — Jul. 2005
  Advisors: Sied Mehdi Fakhraei and Caro Lucas
  Thesis: *Bio-Inspired SoC Implementation of Neural Networks*
- **B.S. in Electrical and Computer Engineering.** University of Tehran — Jul. 2002
  Advisors: Sied Mehdi Fakhraei and Zainalabedin Navabi
  Dissertation: *Cim++: A C++ Library for Object Oriented Hardware Design*

Honors and Awards

- First holder of the Catherine M. and James E. Allchin Early Career Professorship. Georgia Institute of Technology — 2013
- The William Chan Memorial Dissertation Award. Computer Science and Engineering, University of Washington — 2013
- Paper selected for **Communications of the ACM Research Highlights**. "Neural Acceleration for General-Purpose Approximate Programs" — 2013
- Paper selected for **IEEE Micro Top Picks from the 2012 Computer Architecture Conferences**. "Neural Acceleration for General-Purpose Approximate Programs" — 2013
- Paper selected for **Communications of the ACM Research Highlights**. "Power Challenges May End the Multicore Era" — 2012
- Paper selected for **Communications of the ACM Research Highlights**. "Looking Back and Looking Forward: Power, Performance, and Upheaval" — 2012
- Paper selected for **IEEE Micro Top Picks from the 2011 Computer Architecture Conferences**. "Dark Silicon and the End of Multicore Scaling" — 2012
- Paper selected for **IEEE Micro Top Picks from the 2011 Computer Architecture Conferences**. "What Is Happening to Power, Performance, and Software?" — 2012
- Ranked 5^{th} among 5,040 participants of Iran's national M.S. entrance exam. Computer Engineering track — 2002
- Dean's honored graduate. School of Engineering, University of Tehran — 2002
  Ranked 2^{nd} among graduates of the class of 2002
- Faculty of Engineering (FOE) award. University of Tehran, Computer Engineering track — 2001-2002
  Annually awarded to the top three students in each track by School of Engineering
- Best paper award. IEEE student branch paper contest, University of Tehran, "Digital Implementation of Conic Section Function Neural Networks" — 2001

PUBLICATIONS Conference Papers

1. B. Robatmili, D. Li, **H. Esmaeilzadeh**, M. Govindan, A. Smith, A. Putnam, D. Burger, and S. Keckler, "How to Implement Effective Prediction and Forwarding for Fusable Dynamic Multicore Architectures," to appear in *International Symposium on High Performance Computer Architecture (HPCA),* February 2013.
2. **H. Esmaeilzadeh**, A. Sampson, L. Ceze, and D. Burger, "Neural Acceleration for General-Purpose Approximate Programs," in *International Symposium on Microarchitecture (MICRO),* pp. 449–460, December 2012. (**selected for IEEE Micro Top Picks**)
3. **H. Esmaeilzadeh**, A. Sampson, L. Ceze, and D. Burger, "Architecture Support for Disciplined Approximate Programming," in *Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp. 301–312, March 2012.
4. **H. Esmaeilzadeh**, E. Blem, R. St. Amant, K. Sankaralingam, and D. Burger, "Dark Silicon and the End of Multicore Scaling," in *International Symposium on Computer Architecture (ISCA),* pp. 365–376, June 2011. (**selected for Communications of ACM Research Highlights and IEEE Micro Top Picks**)
5. **H. Esmaeilzadeh**, T. Cao, X. Yang, S. Blackburn, and K. McKinley, "Looking Back on the Language and Hardware Revolution: Measured Power, Performance, and Scaling," in *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp. 319–332, March 2011. (**selected for Communications of ACM Research Highlights and IEEE Micro Top Picks**)
6. **H. Esmaeilzadeh**, M.R. Jamali, P. Saeedi, A. Moghimi, C. Lucas, S.M. Fakhraie, "NNEP, Design Pattern for Neural-Network-Based Embedded Systems," in *International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES),* pp. 673-678, June 2007.
7. **H. Esmaeilzadeh**, P. Saeedi, B.N. Araabi, C. Lucas, S.M. Fakhraie, "Neural Network Stream Processing Core (NnSP) for Embedded Systems," in *International Symposium on Circuits and Systems (ISCAS),* pp. 2773-2776, May 2006.
8. **H. Esmaeilzadeh**, E. Ebrahimi, A. Mioghimi, Z. Navabi, C. Lucas, S.M. Fakhraie, "DCim++: A C++ Library for Parallel Distributed Simulation," in *International Symposium on Circuits and Systems (ISCAS),* pp. 1283-1286, May 2006.
9. A. Banaiyan, **H. Esmaeilzadeh**, S. Safari, "Co-Evolutionary Scheduling and Mapping for High-Level Synthesis," in *IEEE International Conference on Engineering of Intelligent Systems,* pp. 1-5, April 2006.
10. **H. Esmaeilzadeh**, F. Farzan, N. Shahidi, S. M. Fakhraie, C. Lucas, Mohammad Tehranipoor, "NnSP: Embedded Neural Networks Stream Processor," in *Midwest Symposium on Circuits and Systems (MWSCAS),* vol. 1, pp. 223-226, August 2005.
11. **H. Esmaeilzadeh**, S. Shamshiri, P. Saeedi, Z. Navabi, "ISC: Reconfigurable Scan-Cell Architecture for Low Power Testing," in *Asian Test Symposium (ATS),* pp. 236-241, December 2005.
12. **H. Esmaeilzadeh**, Z. Navabi, "Cim++: An Object-Oriented Design and Simulation Framework for Education of Hardware/Software Codesign," in *International Conference on Simulation in Education (ICSiE),* January 2005.
13. **H. Esmaeilzadeh**, H. Farshbaf, C. Lucas, S.M. Fakhraie, "Digital Implementation for Conic Section Function Network," in *International Conference on Microelectronics (ICM),* pp. 564-567, December 2004.
14. N. Shahidi, **H. Esmaeilzadeh**, Marziye Abdollahi, Eiman Ebrahimi, C. Lucas, "Self-Adaptive Memetic Algorithm: An Adaptive Conjugate Gradient Approach," in *Conference on Cybernetics and Intelligent Systems (CIS),* pp. 6-11, December 2004.
15. S. Shamshiri, **H. Esmaeilzadeh**, Z. Navabi, "Test Instruction Set (TIS) for High Level Self-Testing of CPU Cores," in *Asian Test Symposium (ATS),* pp. 158-163, November 2004.
16. S. Shamshiri, **H. Esmaeilzadeh**, M. Alisafaee, P. Lotfikamran and Z. Navabi, "Test Instruction Set (TIS): An Instruction Level CPU Core Self-Testing Method," in *European Test Symposium (ETS),* pp. 15-16, May 2004.
17. S. Safari, **H. Esmaeilzadeh**, A.H. Jahangir, "Testability Improvement during High-Level Synthesis," in *Asian Test Symposium (ATS),* p. 505, November 2003.
18. S. Safari, **H. Esmaeilzadeh**, A.H. Jahangir, "A Novel Improvement Technique for High-Level Test Synthesis," in *International Symposium on Circuits and Systems (ISCAS),* pp. V609-V612, May 2003.

Journal Papers

1. **H. Esmaeilzadeh**, A. Sampson, L. Ceze, and D. Burger, "Neural Acceleration for General-Purpose Approximate Programs," to appear in *Communications of the ACM Research Highlights*. (invited, original at MICRO'12)
2. **H. Esmaeilzadeh**, A. Sampson, L. Ceze, and D. Burger, "Neural Acceleration for General-Purpose Approximate Programs," in *IEEE Micro Top Picks from the 2012 Computer Architecture Conferences*, vol. 33, no. 3, pp. 16–27, May/June 2013. (original at MICRO'12)
3. **H. Esmaeilzadeh**, E. Blem, R. St. Amant, K. Sankaralingam, and D. Burger, "Power Challenges May End the Multicore Era," to appear in *Communications of the ACM Research Highlights*, vol. 56, no. 2, February 2013. (invited, original at ISCA'11)
4. E. Blem, **H. Esmaeilzadeh**, R. St. Amant, K. Sankaralingam, and D. Burger, "Multicore Model from Abstract Single Core Inputs," in *Computer Architecture Letters*, vol. PP, no. 99, pp. 1–3, August 2012.
5. **H. Esmaeilzadeh**, E. Blem, R. St. Amant, K. Sankaralingam, and D. Burger, "Power Limitations and Dark Silicon Challenge the Future of Multicore," in *ACM Transactions on Computer Systems (TOCS)* vol. 30, no. 3, pp. 11:1–11:27, August 2012. (invited)
6. **H. Esmaeilzadeh**, E. Blem, R. St. Amant, K. Sankaralingam, and D. Burger, "Dark Silicon and the End of Multicore Scaling," in *IEEE Micro Top Picks from the 2011 Computer Architecture Conferences*, vol. 32, no. 3, pp. 122–134, May/June 2012. (original at ISCA'11)
7. **H. Esmaeilzadeh**, T. Cao, X. Yang, S. Blackburn, and K. McKinley, "Looking Back and Looking Forward: Power, Performance, and Upheaval," in *Communications of the ACM Research Highlights*, vol. 55, no. 7, pp. 105–114, May/June 2012. (invited, original at ASPLOS'11)
8. **H. Esmaeilzadeh**, T. Cao, X. Yang, S. Blackburn, and K. McKinley, "What Is Happening to Power, Performance, and Software?," in *IEEE Micro Top Picks from the 2011 Computer Architecture Conferences*, vol. 32, no. 3, pp. 110–121, May/June 2012. (original at ASPLOS'11)
9. S. Safari, A. H. Jahangir, **H. Esmaeilzadeh**, "A Parameterized Graph-Based Framework for High-level Test Synthesis," *Integration, the VLSI Journal,* vol. 39, no. 4, pp. 363–381, July 2006.
10. S. Shamshiri, **H. Esmaeilzadeh**, Z. Navabi, "Instruction-Level Test Methodology for CPU Core Self-Testing," in *special issue of ACM Transactions on Design Automation of Electronic Systems (TODAES) on "Design Validation of Large Systems,"* vol. 10, no. 4, pp. 673–689, October 2005.
11. N. Shahidi, **H. Esmaeilzadeh**, M. Abdollahi, C. Lucas, "Memetic Algorithm Based Path Planning for a Mobile Robot," in *International Journal of Information Technology,* vol. 1, no. 4, pp. 174–177, 2004.
12. **H. Esmaeilzadeh**, N. Shahidi, E. Ebrahimi, A. Moghimi, C. Lucas, Z. Navabi, "Cim++: A C++ Library for Object Oriented Hardware Design," in *International Journal of Science and Information Technology (IJSIT), Lecture Notes of 1st International Conference on Informatics*, vol. 1, no. 2, pp. 35–41, September 2004.

Workshop Papers

1. **H. Esmaeilzadeh**, A. Sampson, M. Ringenburg, L. Ceze, D. Grossman, and D. Burger, "Addressing Dark Silicon Challenges with Disciplined Approximate Computing," in *The First Workshop on Dark Silicon (DaSi) held in conjunction with ISCA,* June 2012.
2. **H. Esmaeilzadeh**, A. Sampson, L. Ceze, and D. Burger, "Towards Neural Acceleration for General-Purpose Approximate Computing," in *The Forth Workshop on Energy-Efficient Design (WEED) held in conjunction with ISCA,* June 2012.
3. **H. Esmaeilzadeh**, S. Girbal, K. McKinley, O. Temam, and S. Yehia, "Programming Heterogeneous Hardware Components with Software Components," in *The Sixth Workshop on SoC Architecture, Accelerators and Workloads (SAW) held in conjunction with HPCA,* February 2011.
4. **H. Esmaeilzadeh**, S. Blackburn, X. Yang, and K. McKinley, "Power and Performance of Native and Java Benchmarks on 130nm to 32nm Process Technologies," *Sixth Annual Workshop on Modeling, Benchmarking and Simulations (MOBS) held in conjunction with ISCA,* June 2010.
5. **H. Esmaeilzadeh** and D. Burger, "Hierarchical Control Flow Speculation: Support for Aggressive Predication," in *The 2009 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA) held in conjunction with ISCA 2009*, pp. 71–80, June 2009.

6. **H. Esmaeilzadeh**, S. Shamshiri, P. Saeedi, E. Ebrahimi, A. Pedram, Z. Navabi, "Interleaved Scan-Cell Architecture for Low Power Test," in *Fifth Workshop on Register Transfer level Test (WRTLT),* pp. 123–128, November 2004.
7. M. Alisafaee, P. Lotfi, S. Shamshiri, **H. Esmaeilzadeh**, A. Pedram, Z. Navabi, "MCBIST: A New Online BIST Scheme," in *Fifth Workshop on Register Transfer level Test (WRTLT),* pp. 85-90, November 2004.
8. S. Shamshiri, **H. Esmaeilzadeh**, Z. Navabi, "TIS: An Instruction Level Test Methodology for CPU Core Software-Based Self-Testing," in *International High Level Design Validation and Test Workshop (HLDVT),* pp. 25-29, November 2004.
9. S. Safari, **H. Esamaeilzadeh**, A.M. Jahangir, "A Novel Register Allocation Method For Testability Improvement," in *The Forth Workshop on RTL and High Level Testing (WRTLT),* November 2003.

Patent

Doug Burger, Stephen W. Keckler, **Hadi Esmaeilzadeh**, "Method, System and Computer-Accessible Medium for Providing a Distributed Predicate Prediction," U.S. Patent 8,433,885, Filed September 9, 2009, Issued April 22, 2013.

Research Experience

- **Principal investigator.** *Alternative Computing Technologies (ACT) Lab* Aug. 2013–date
  Georgia Institute of Technology
- **Research assistant.** *Safe MultiProcessing Architectures (SAMPA) Lab* Sep. 2010–Aug. 2013
  University of Washington
  Advisors: Doug Burger and Luis Ceze

  Neural processing units. *As part of the broader approximate computing effort in the group, I founded the NPU project. I proposed a new acceleration technique that leverages a simple programmer annotation ("approximable") to transform a hot code region from a von Neumann model to a neural model [MICRO'12].*

  Variable-precision architectures. *I led the research on architecture support for disciplined approximate programming. I introduced a variable-precision Instruction Set Architecture (ISA) that allows conventional Von Neumann processors to interleave approximate and precise instructions. I also designed the dual-voltage Truffle microarchitecture that implements the ISA [ASPLOS'12].*

  Dark silicon and multicore scaling. *I led the Dark Silicon project that I challenged the conventional wisdom that multicore scaling—increasing the number of cores every new technology generation–is the right path for exploiting increased transistor counts and sustaining the historical performance trends [ISCA'11].*
- **Summer intern.** *Extreme Computing Group (XCG)* Jun. 2012–Sep. 2012
  Microsoft Research
  Mentor: Doug Burger

  ISA support for neural networks. *I studied the ISA extensions and microarchitectural mechanisms that improves evaluation of neural networks on conventional processors both with and without SIMD support.*

  Analog neural networks. *I also implemented a high-level simulator to explore the design space of analog neural networks. With this tool, I studied the accuracy requirements of the analog neural networks and their energy efficiency compared to their digital counterparts.*
- **Research assistant.** *Computer Architecture and Technology (CART) Lab* Sep. 2006–Aug. 2010
  The University of Texas at Austin
  Advisors: Doug Burger and Kathryn McKinley

  Measured power and modern workloads. *I studied the interplay between two revolutions, (1) the rise of multiprocessors and (2) the rise of managed programming languages, by measuring power, performance, energy, and effects of technology scaling on real hardware [ASPLOS'11].*

  Distributed predicate prediction. *I designed a distributed predicate predictor that enables composable dynamic multicores to efficiently run heavily predicated code [HPCA'13]. Our patent application on the design is pending.*
- **Research assistant.** *Silicon Intelligence (SI) Lab* Sep. 2004–Jun. 2006
  University of Tehran
  Advisors: Sied Mehdi Fakhraie and Caro Lucas

  Neural networks IP core. *For my master's thesis project, I worked on providing a holistic and reusable solution for integrating and using neural hardware in SoC and SoPC-based embedded systems [ISCAS'06].*

- **Research assistant.** *Computer Aided Design (CAD) Lab* Sep. 2002–Aug. 2004
  University of Tehran
  Advisor: Zainalabedin Navabi
  Interleaved scan cell. *I designed a novel flip-flop architecture to mask the scan chain shift operations from the rest of the design to reduce power dissipation during test [ATS'05].*
  Test instruction set. *We proposed the test instruction set that allows processor cores to self-test their circuitry while executing applications by utilizing wasted processor cycles [TODAES'05].*
- **Undergraduate research assistant.** *Computer Aided Design (CAD) Lab* Jun. 2002–Aug. 2002
  University of Tehran
  Advisor: Zainalabedin Navabi
  Test-aware high-level synthesis. *I implemented a full-fledged test-aware high-level synthesis tool that started from DFGs and generated synthesizable Verilog code [VLSI'06].*
- **Undergraduate research assistant.** *VLSI Circuits and Systems Lab* Jun. 2001–May 2002
  University of Tehran
  Advisoris: Sied Mehdi Fakhraie and Zainalabedin Navabi
  Object-oriented hardware design. *I designed and implemented the Cim++ library [IJSIT'04] that provides the necessary constructs to use C++ for object-oriented hardware-software co-design. I later extended Cim++ with MPI and built a distributed circuit simulator, called DCim++ [ISCAS'06].*
  Hardware neural network. *As my very first research project, I designed and synthesized a digital conic section function neural network for the handwritten digit pattern recognition task [ICM'04].*

Teaching Experience

- **Teaching assistant.** Held office hours, answered email/newsgroup queries, led review sessions, designed and graded student homework.

CSE467: Advanced Logic Design. University of Washington	Winter 2011
CSE401: Introduction to Compiler Construction. University of Washington	Autumn 2010
CS380C: Advanced Compiler Techniques (graduate-level). The University of Texas at Austin	Fall 2009
CS345: Programming Languages. The University of Texas at Austin	Spring 2009
ECE365: Advanced VLSI Design (graduate-level). University of Tehran	Fall 2004
ECE624: ASIC Design (graduate-level). University of Tehran	Spring 2004
ECE446: VLSI Design. University of Tehran	Fall 2003
ECE445: Digital Electronics. University of Tehran	Spring 2003
ECE423: Computer Architecture. University of Tehran	Fall 2002
ECE367: Digital Logic Circuits. University of Tehran	Spring 2001–Spring 2002
ECE207: Microprocessors. University of Tehran	Fall 2001
ECE303: Computer Workshop. University of Tehran	Fall 1999

- **Instructor.** Designed course, gave lectures, held office hours, answered email/newsgroup queries, designed and graded homework and exams.
  Introduction to Communication Networks. University of Tehran, IT education series for professionals with no computer science background. Summer 2003

Professional Activities

- **Program Committee Member.**

ACM International Conference on Computing Frontiers (CF)	2014
International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)	2013

- **Reviewer.**

IEEE International Symposium on High Performance Computer Architecture (HPCA)	2014
International Symposium on Microarchitecture (MICRO)	2013
IEEE Micro Magazine (Micro)	2013
IEEE Transactions on Computers (TC)	2013
IEEE International Symposium on High Performance Computer Architecture (HPCA)	2013

ACM Transactions on Architecture and Code Optimization (TACO)	2012
International Symposium on Computer Architecture (ISCA)	2010
Elsevier Journal of Decision Support Systems (DSS)	2009
International Conference on Supercomputing (ICS)	2009
International Conference for High Performance Computing, Networking, Storage and Analysis (SC)	2007

- **Member.** ACM and IEEE

Work Experience

- **Manager.** Hardware–Software integration group, SiNA Microelectronics — Nov. 2004–May 2006
  I managed the team that developed embedded system software for small office-home office (SOHO) networking SoCs.
- **Network administrator.** VLSI Circuits and Systems Lab, University of Tehran — Oct. 2001–Jul. 2002

Musical Experience

- **Guest percussionist.** *Tonbak* (Persian goblet drum) and *daf* (chained Persian frame drum)
  Concert in Dashti*. Bereket UT-Austin Middle Eastern Ensemble, Butler School of Music, The University of Texas at Austin, Bates Concert Hall — Apr. 2010
- **Percussionist.** *Tonbak* and *daf*

Concert in Esfahan* and Mahoor*. Indian and Persian Music Night, The University of Texas at San Antonio, Richard S. Liu Auditorium	Feb. 2010
Concert in Nava* and Esfahan*. The University of Texas at Austin	Dec. 2009
Concert in Mahoor*. The University of Texas at Austin	Mar. 2009
Concert in Chahargah*. University of Tehran, Chamran Auditorium	May 2006
Concert in Rast-Panjgah* and Nava*. University of Tehran, Chamran Auditorium	May 2005
Concert in Shoor*. University of Tehran, Chamran Auditorium	May 2004

References

- **Doug Burger.** Director, Microsoft Research — dburger@microsoft.com
  One Microsoft Way, Building: B115, Redmond, WA 98052 — +1 (425) 538-1668
- **Luis Ceze.** Associate Professor, University of Washington — luisceze@cs.washington.edu
  University of Washington Box 352350, Seattle, WA 98195 — +1 (206) 543-1896
- **Babak Falsafi.** Professor, Ecole Polytechnique Federale de Lausanne — babak.falsafi@epfl.ch
  INJ 233, Station 14, CH-1015 Lausanne, Switzerland — +41 (21) 693-5592
- **Mark Hill.** Professor, University of Wisconsin-Madison — markhill@cs.wisc.edu
  1210 West Dayton St., Madison, WI 53706 — +1 (608) 262-2196
- **Kathryn McKinley.** Principal Researcher, Microsoft Research — mckinley@cs.utexas.edu
  One Microsoft Way, Building: B99, Redmond, WA 98052 — +1 (512) 232-7891
- **Karu Sankaralingam.** Associate Professor, University of Wisconsin-Madison — karu@cs.wisc.edu
  1210 West Dayton St., Madison, WI 53706 — +1 (608) 890-0121

* One of the twelve musical modal systems in traditional Persian music.