## CS4290/CS 6290 High-Performance Computer Architecture

School of Computer Science  
Georgia Institute of Technology

### Instructor: Prof. Hyesoon Kim  
### TA: Aemen Lodhi

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<td></td>
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<tr>
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<td></td>
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<tr>
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<tr>
<td></td>
<td>10/2</td>
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<tr>
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<td></td>
<td>App A</td>
<td>Mid-term</td>
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<tr>
<td></td>
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<tr>
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</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>10</td>
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<td>Ch5/App C</td>
<td></td>
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<tr>
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<td>10/30</td>
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<tr>
<td>12</td>
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<td>Ch4</td>
<td></td>
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<tr>
<td></td>
<td>11/6</td>
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<tr>
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<tr>
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<tr>
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<td></td>
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<td></td>
<td>11/27</td>
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<td></td>
</tr>
<tr>
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<td>Review session</td>
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<td></td>
<td>Project due</td>
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<td>Final</td>
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<td>Final exam</td>
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