CS4803DGC Design Game Consoles

Spring 2009

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Georgia Tech | College of Computing
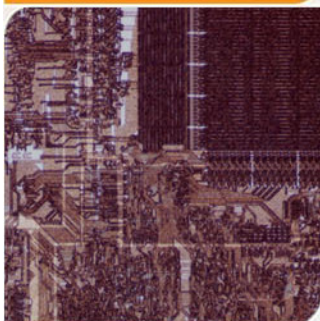
The ARM9 Family-High Performance Microprocessors for Embedded Applications

Nintendo DS/DSi/ DSlite

Hardware Picture

Wireless LAN RF transceiver IC (RF Micro Devices)

Interface connector for upper LCD display (51 pins)

Connection to AC adapter

Wireless communication MAC/baseband processing IC (Mitsumi Electric)

Microcontroller

32Mbit FCRAM

Connection to Li-ion rechargeable battery

RF bandpass filter

Operating switches

Operating switches

Crystal oscillator

IC SAW filter

C/NTR-CPU-01

Large-capacity type wound inductor (probably Taiyo Yuden or TDK)

Power supply or audio control IC (Mitsumi Electric)

Game Boy Advance cartridge connector

Volume dial

Headphone/microphone jack

Interface connector for lower LCD display (45 pins)

Fig 1 Key Circuitry Clumped on One Side The photo is close to the actual size – 141 x 76mm (longest area). The wireless module and microcontroller were covered by a metal shielding plate.

http://www.cosc.brocku.ca/Offerings/3P92/seminars/nintendo_ds_slideshow.pdf
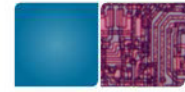
Hardware Specifications

- Dual TFT LCD screens
- CPUs
  - ARM 7 TDMI (33MHz)
  - ARM 9 946E-S (67MHz)
- Main memory: 4MB RAM
  - VRAM: 656 KiB
- 2D graphics
 - Up to 4 backgrounds
- 3D graphics

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ARM7/ARM9

- Both can be running code at the same time.

- ARM 7 is the only CPU that controls the touch screen.

  - Interrupt based

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Brief History of ARM

- ARM is short for Advanced Risc Machines Ltd.
  - Founded 1990, owned by Acorn, Apple and VLSI
- Known before becoming ARM as computer manufacturer
- ARM is one of the most licensed company
- Used especially in portable devices due to low power consumption and reasonable performance (MIPS/watt)
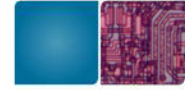
ARM7 and ARM7 TDMI

- ARM7: 3 stage pipeline, 16 32-bit Registers , 32-bit instruction set
- TMDI
  - Thumb instruction set
  - Debug-interface
  - Multiplier (hardware)
  - Interrupt (fast interrupt)
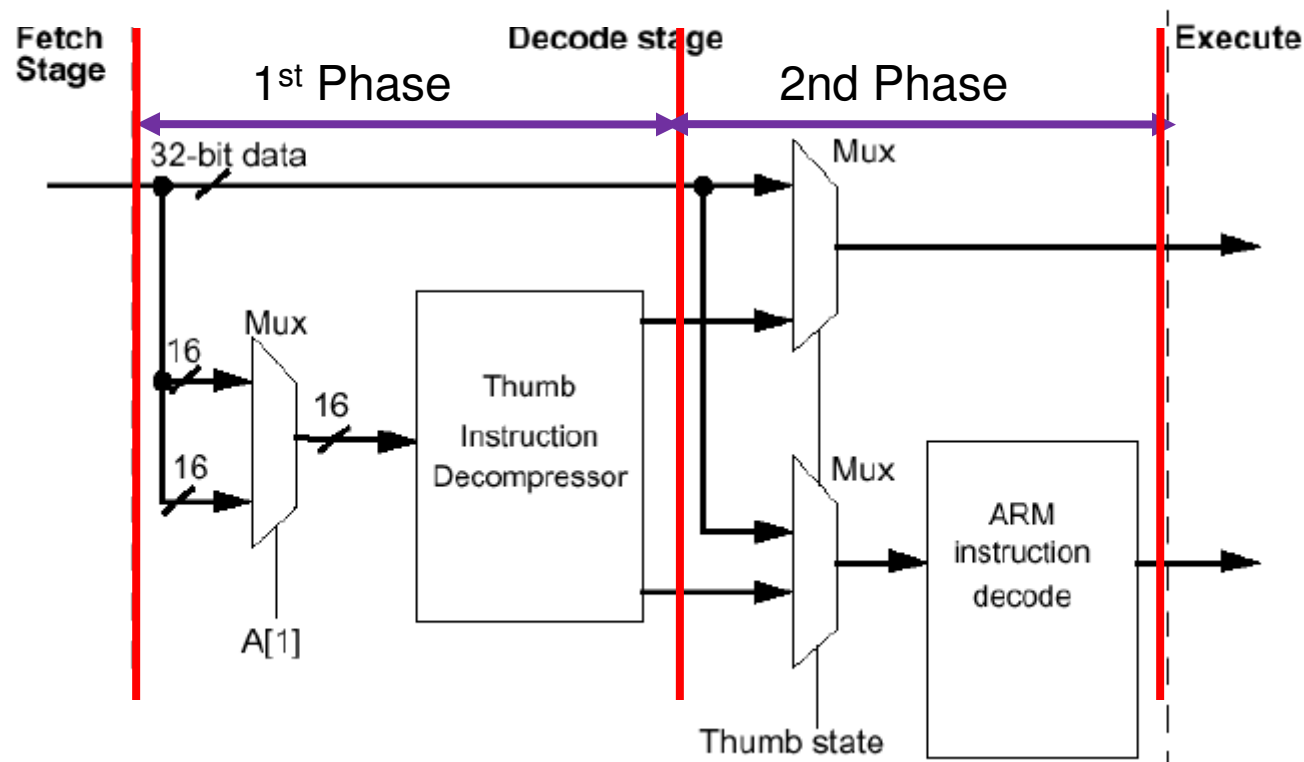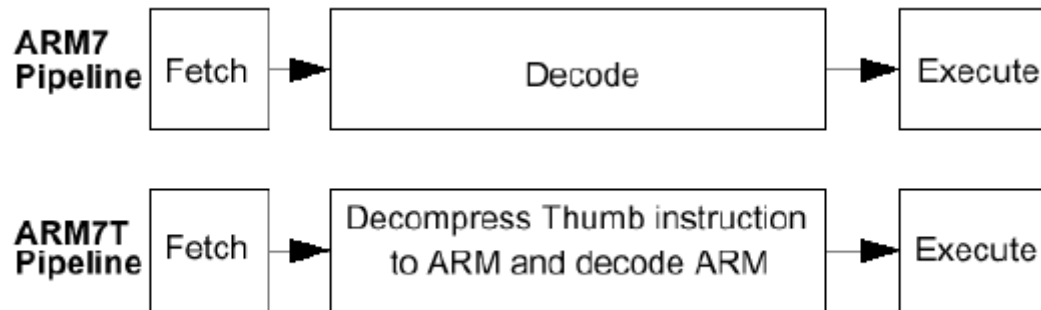 - The most commonly used one

ARM7 TDMI

- 32/16-bit RISC
- 32-bit ARM instruction set
- 16-bit Thumb instruction set
- 3-stage pipeline
- Very small die size and low power
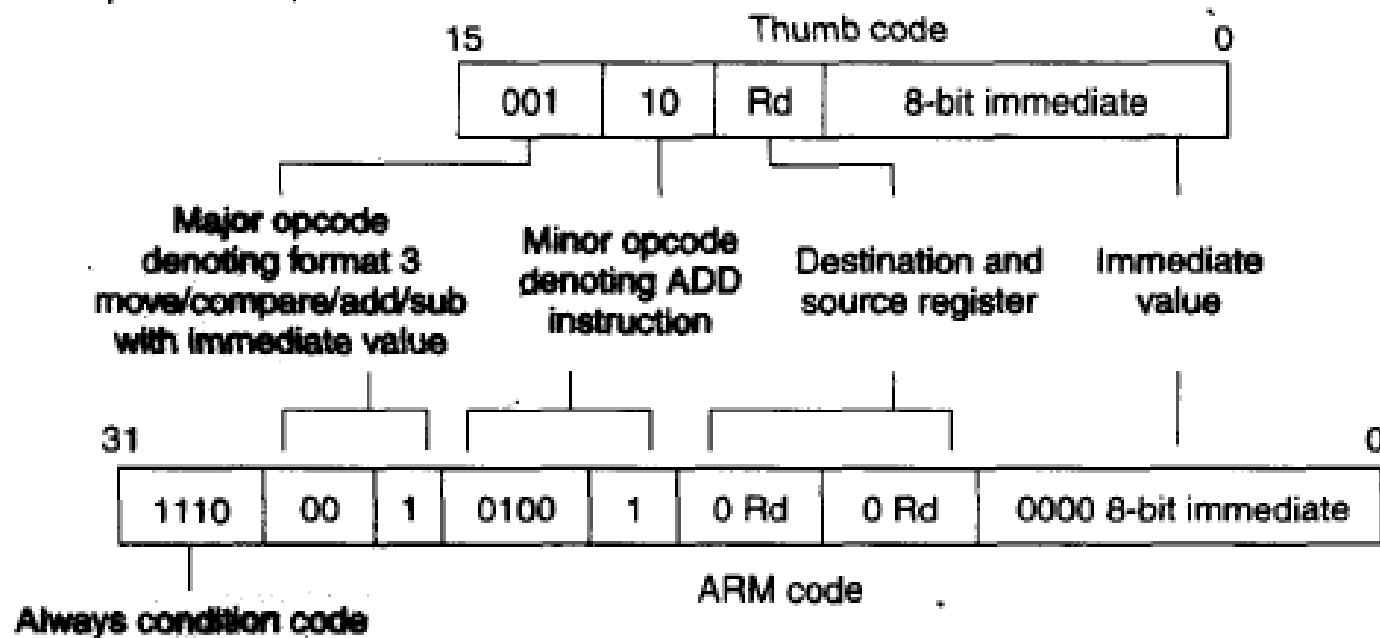- Unified bus interface (32-bit data bus carries both instruction, data)
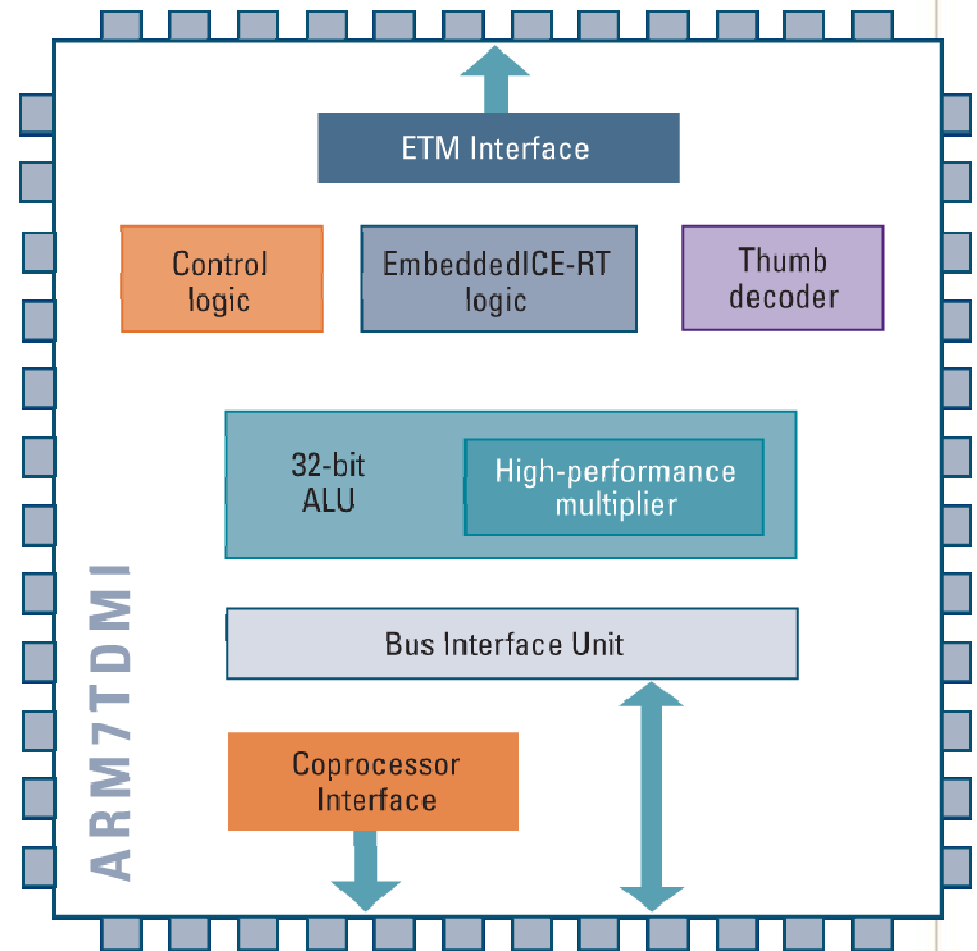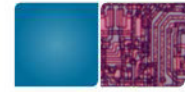
Thumb Instruction Decode

Thumb Instruction

Example: ADD rd, #Constant

- Instruction compression to save I-cache/memory accesses
- Use only top 8 registers,
- 3 operands → 2 operands

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Thumb…

- Instructions are compiled either native ARM code or Thumb code
  - To utilize full 16bit opcode
 - Use current processor status register (CPSR) to set thumb/native instruction

ARM Instruction Set

- All instructions are conditional

- BX, branch and eXhange → branch and exchange (Thumb)

- Link register (subroutine Link register)
  - R14 receives the return address when a Branch with Link (BL or BLX) instruction is executed

ARM9

- 5-stage pipeline
- I-cache and D-cache
- Floating point support with the optional VFP9-S coprocessor
- Enhanced 16 x 32-bit multiplier capable of single cycle MAC operations
- The ARM946E-S processor supports ARM's real-time trace technology
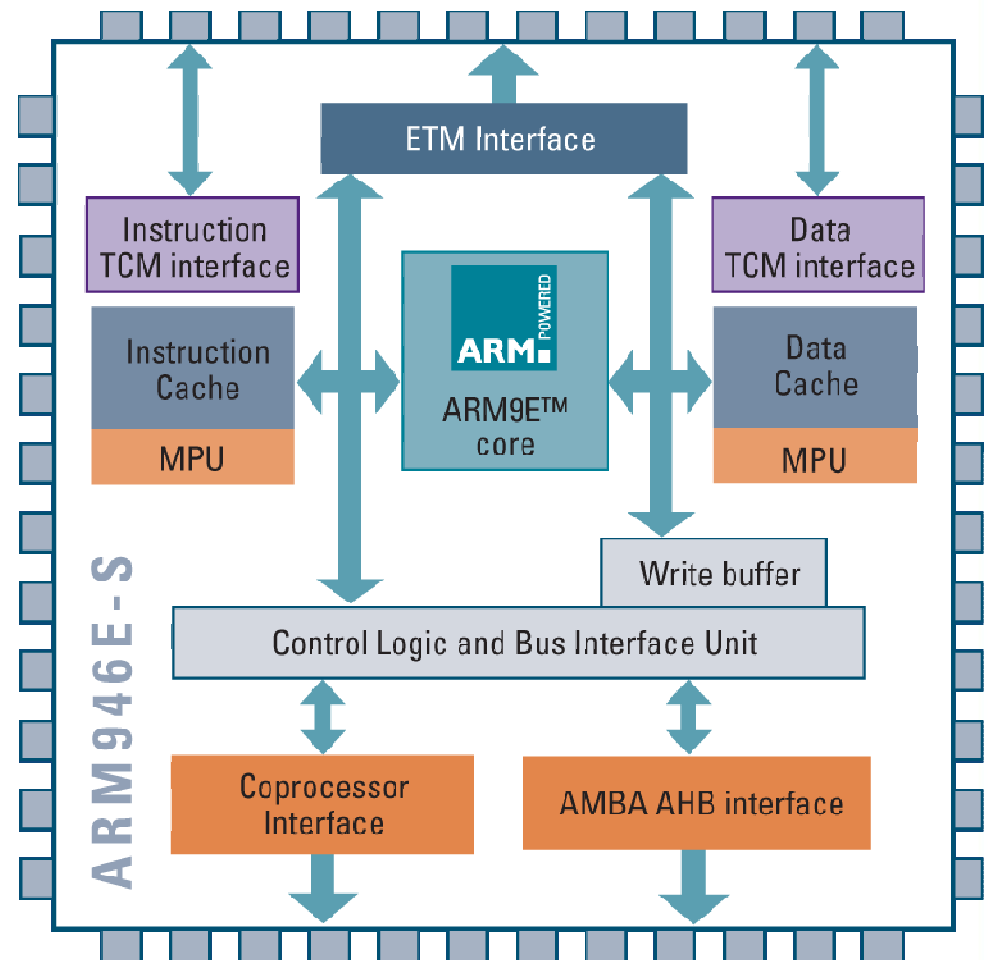
ARM946E-S

- Embedded Core with Flexible Cached Memory System & DSP Instruction Set Extensions
- Memory Protection Unit (MPU) supporting all major RTOS: Vxworks, pSOS
- Flexible instruction and data cache sizes
- 180nm → 90nm
- Imaging products
  - Printers, digital cameras
- Networking systems
- Automotive control

ARM9

- ## ARM7 3stage->ARM9 5 stage

  – Increase clock frequency

ARM7TDMI Pipeline Operation

Fetch	Decode		Execute
Instruction Fetch	Convert Thumb to ARM	Main Decode Register Address Decode	Register Read Shifter ALU Writeback

ARM9TDMI Pipeline Operation

Fetch	Decode	Execute	Memory	Writeback
Instruction Fetch	ARM Decode Reg. Address Register Decode Read - - - - - - - - - - - - - - - Thumb Decode Reg. Address Register Decode Read	Shifter ALU	Memory Data access	ALU Result and / or Load data Writeback

ARM9 Pipeline

- ARM7: Thumb instruction decode: first ½ phase of decode stage
- ARM9: Parallel decoding
- ARM7: ALU (arithmetic, and logic units) is active all the time
- ARM9: Two units are partitioned to save power
- ARM9: Forwarding path

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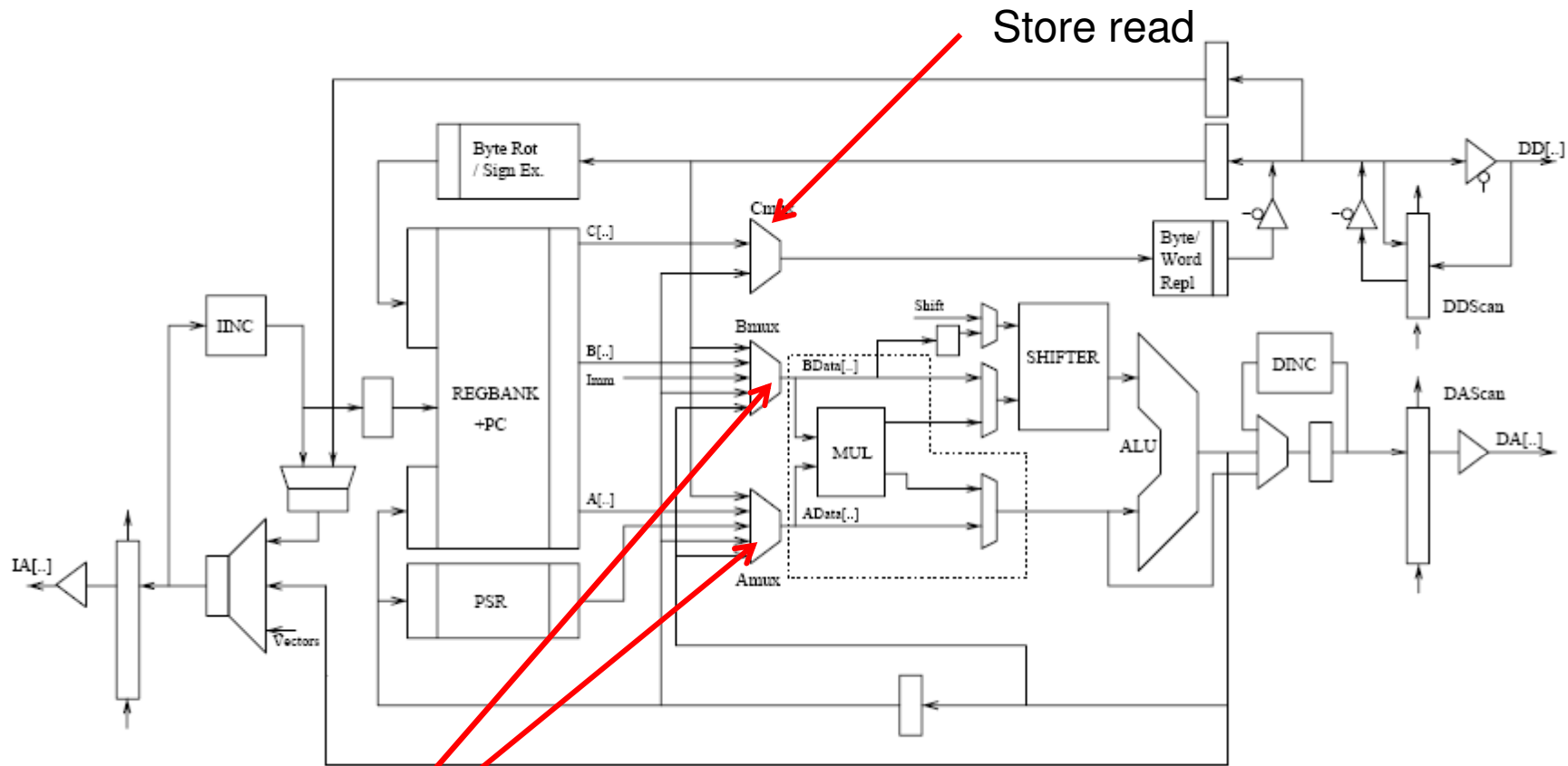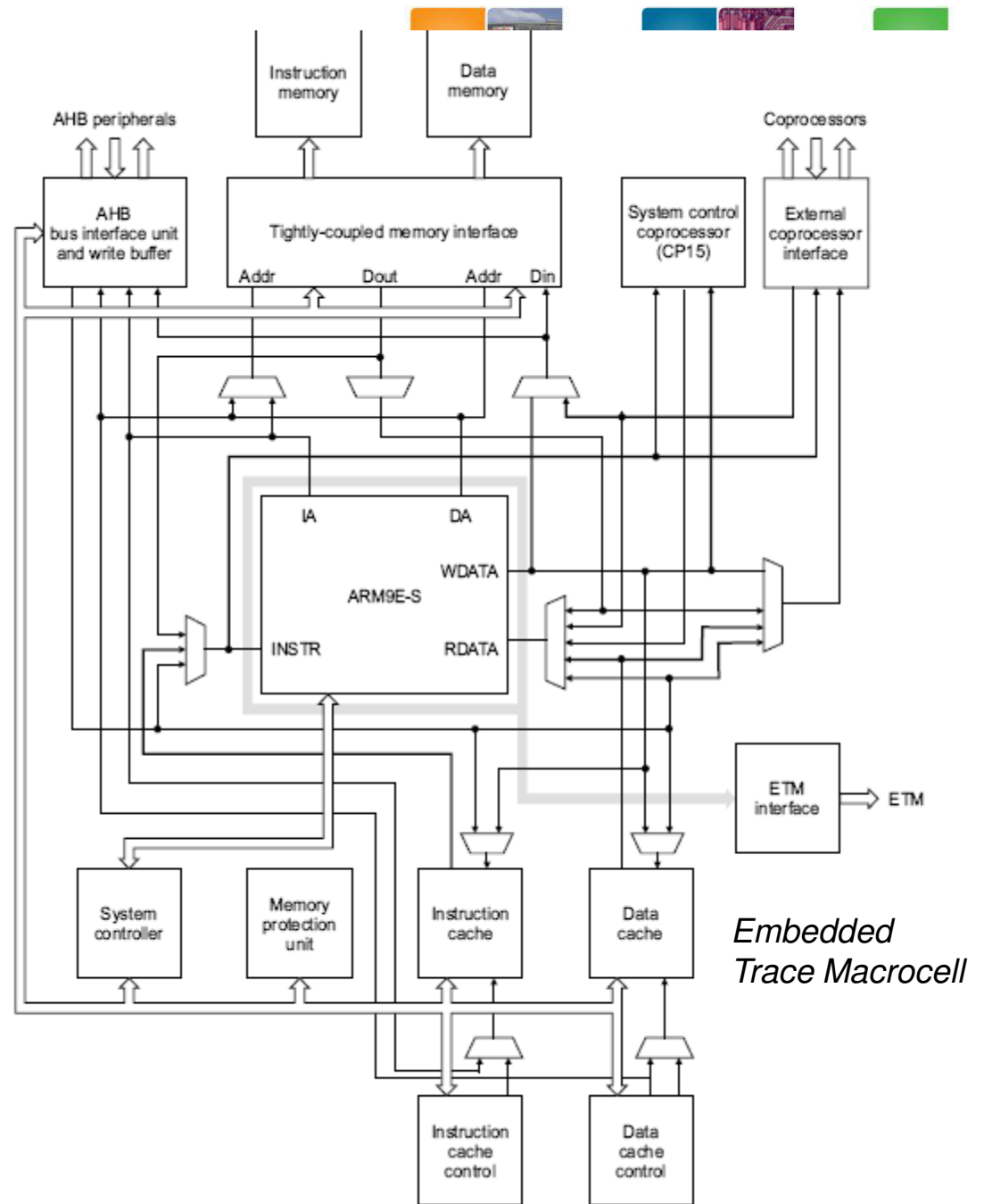# ARM9 TDMI Datapath

Store read

Figure 2 : The ARM9TDMI Datapath

- 3 register read ports and two write ports
  - 2 read: execution unit 1 read: store data during execution stage (no latch)

ARM946E-S

AHB peripherals

Instruction memory

Data memory

Coprocessors

AHB bus interface unit and write buffer

Tightly-coupled memory interface

Addr   Dout   Addr   Din

System control coprocessor (CP15)

External coprocessor interface

IA   DA

WDATA

ARM9E-S

INSTR   RDATA

ETM interface → ETM

System controller

Memory protection unit

Instruction cache

Data cache

Embedded Trace Macrocell

Instruction cache control

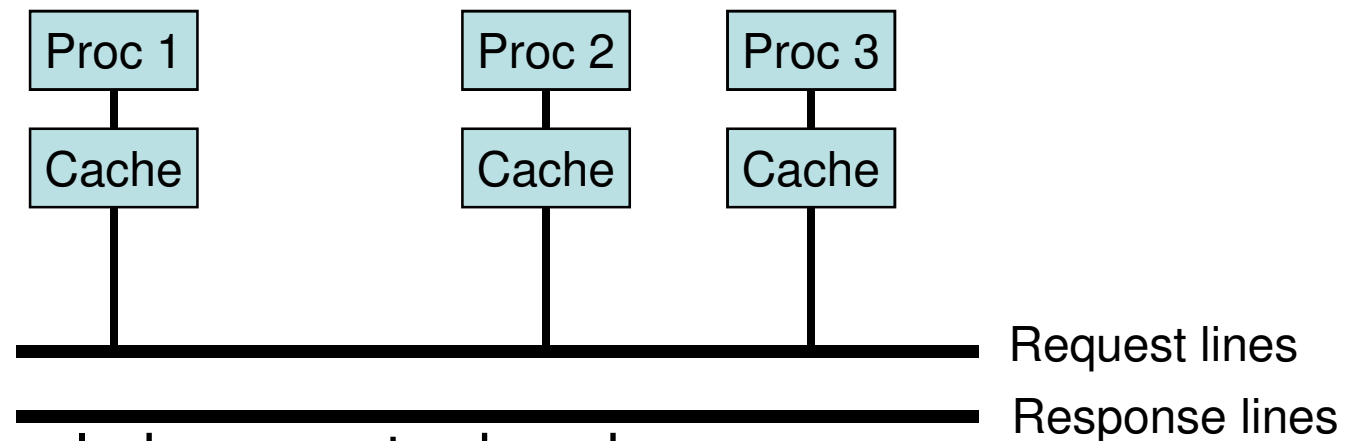Data cache control

AHB (Advanced High-performance Bus)

- single clock edge operation (rising edge)
- unidirectional (nontristate) buses
- burst transfers
- split transactions:
  - Request (address) and Reply (data)

- single-cycle bus master handover

ETM (Embedded Trace Macrocells)

- Help Debugging and trace facilities
- Capture both before and after a specific event of processor's state
- Can be configured by software
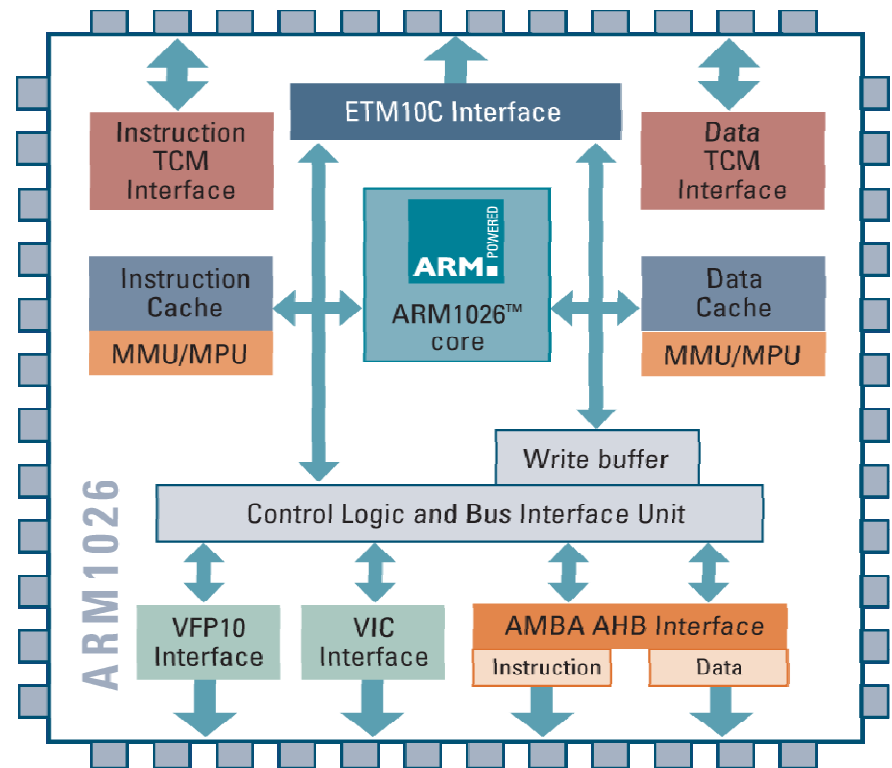- Help code development

Realview trace

ARM10E

- A Jazelle Technology enhanced 32-bit RISC
  - Jazelle Technology: execute java byte code in hardware
- Support 64bit data
- 16-bit fixed point DSP instructions to enhance performance of many signal processing algorithms

ARM11 MP Core

- Multicore
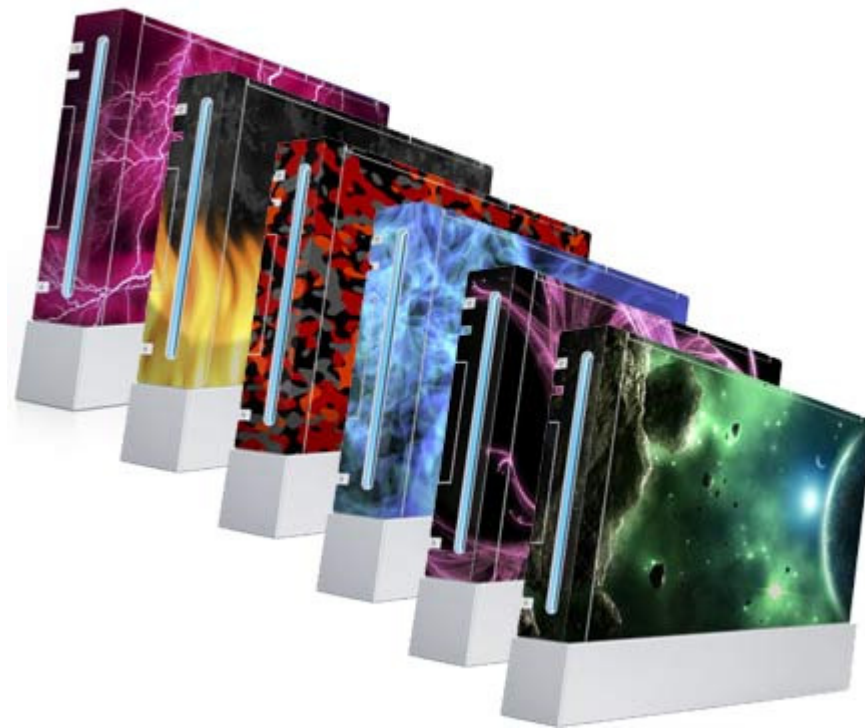- A fully coherent data cache
- High memory bandwidth (1.3GB/s)

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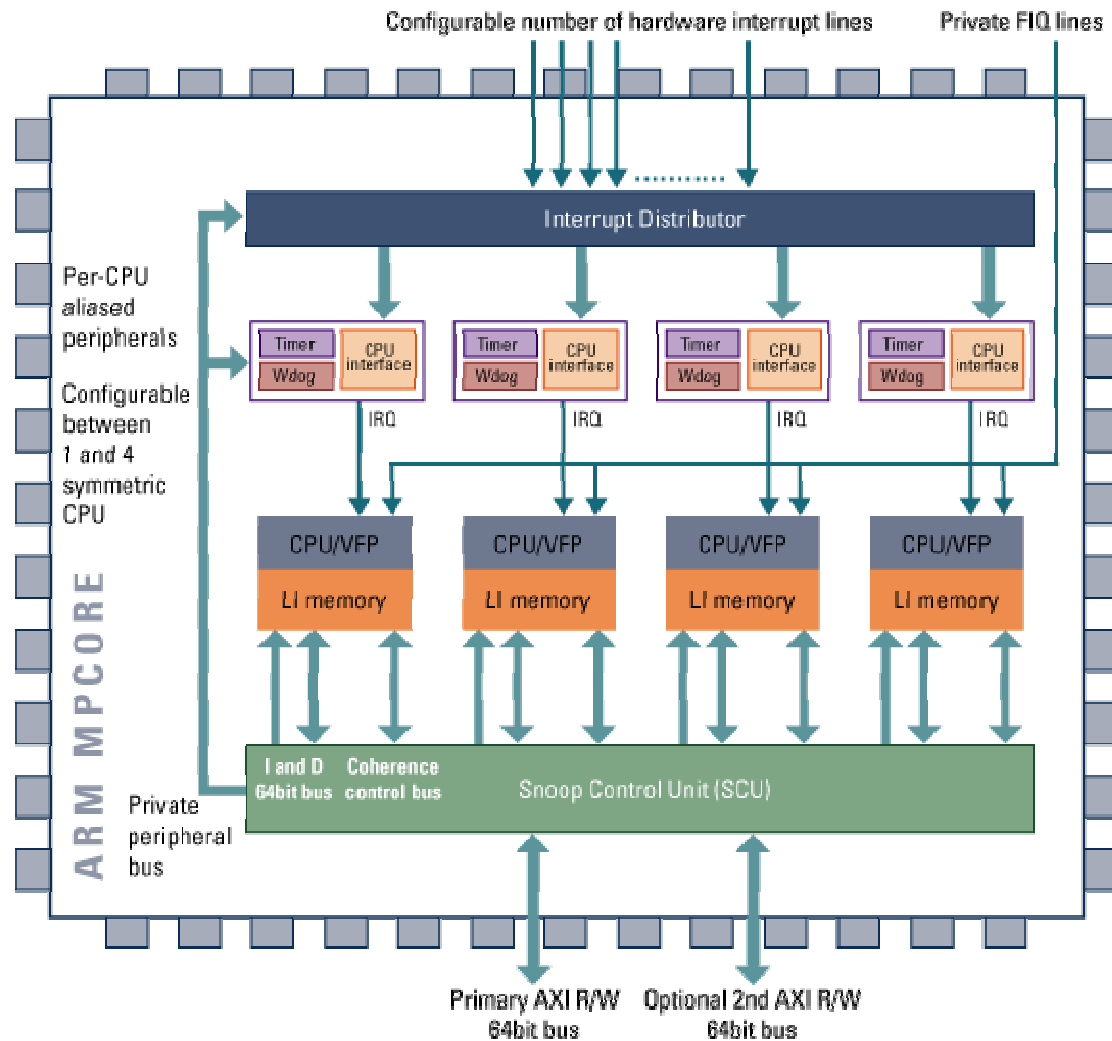
ARM Architecture Feature Comparisons

Feature	ARM9E™	ARM10E™	Intel® XScale™	ARM11™
Architecture Pipeline Length	ARMv5TE(J) 5	ARMv5TE(J) 6	ARMv5TE 7	ARMv6 8
Java Decode	(ARM926EJ)	(ARM1026EJ)	No	Yes
V6 SIMD Instructions	No	No	No	Yes
MIA Instructions	No	No	Yes	Available as coprocessor
Branch Prediction	No	Static	Dynamic	Dynamic
Independent Load-Store Unit	No	Yes	Yes	Yes
Instruction Issue	Scalar, in-order	Scalar, in-order	Scalar, in-order	Scalar, in-order
Concurrency	None	ALU/MAC, LSU	ALU, MAC, LSU	ALU/MAC, LSU
Out-of-order completion	No	Yes	Yes	Yes
Target Implementation	Synthesizable	Synthesizable	Custom chip	Synthesizable and Hard macro
Performance Range	Up to 250MHz	Up to 325MHz	200MHz – >1GHz	350MHz - >1GHz

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Nintendo Wii

Unofficial Diagram

Note: All addresses are physical. For most addresses, add +0x8000000 for RAM or 0xC0000000 for I/O to get logical address on PPC side.

1000000-12FFFFFF
1000000-13FFFFFF

64MB GDDR3 RAM

A/V controller

"Hollywood"

24MB SRAM
00000000-017FFFFF

GPU 0c0xxxxx

DSP 0c005xxx

AHB

0d04xxxx
ehci?

PowerPC 750CL CPU ("Broadway")

A0-A31

D0-D63

Memory/IO bridge

OTP

"Starlet" NEC ARM926 SOC

0d01xxxx
NAND interface

512MB NAND Flash

Note: depending on mode, 0d8 addresses may be remapped to 0d0, cc0 or cd0.

SEEPROM

0d8xxxxx

0d800xxx
GPIO/IPC

DRAM ctrl

0d02
AES

0d03
SHA

0d07xxxx
SDIO interface

SD card slot

0d08xxxx
mini PCI

WiFi module

APB

GC Font ROM / RTC

0d8068xx
GC EXI bus

0d8060xx
Drive Interface

0d8064xx
GC Serial Interface

0d05 USB 0d06
Controllers
oh0 | oh1

GC Mem Card slots (2)

Disc drive

GC controller ports (4)

BT module

External USB ports

Waikiki debug adapter?

USB / SD Gecko

bushing / hackmii.com

USB Ethernet adapter
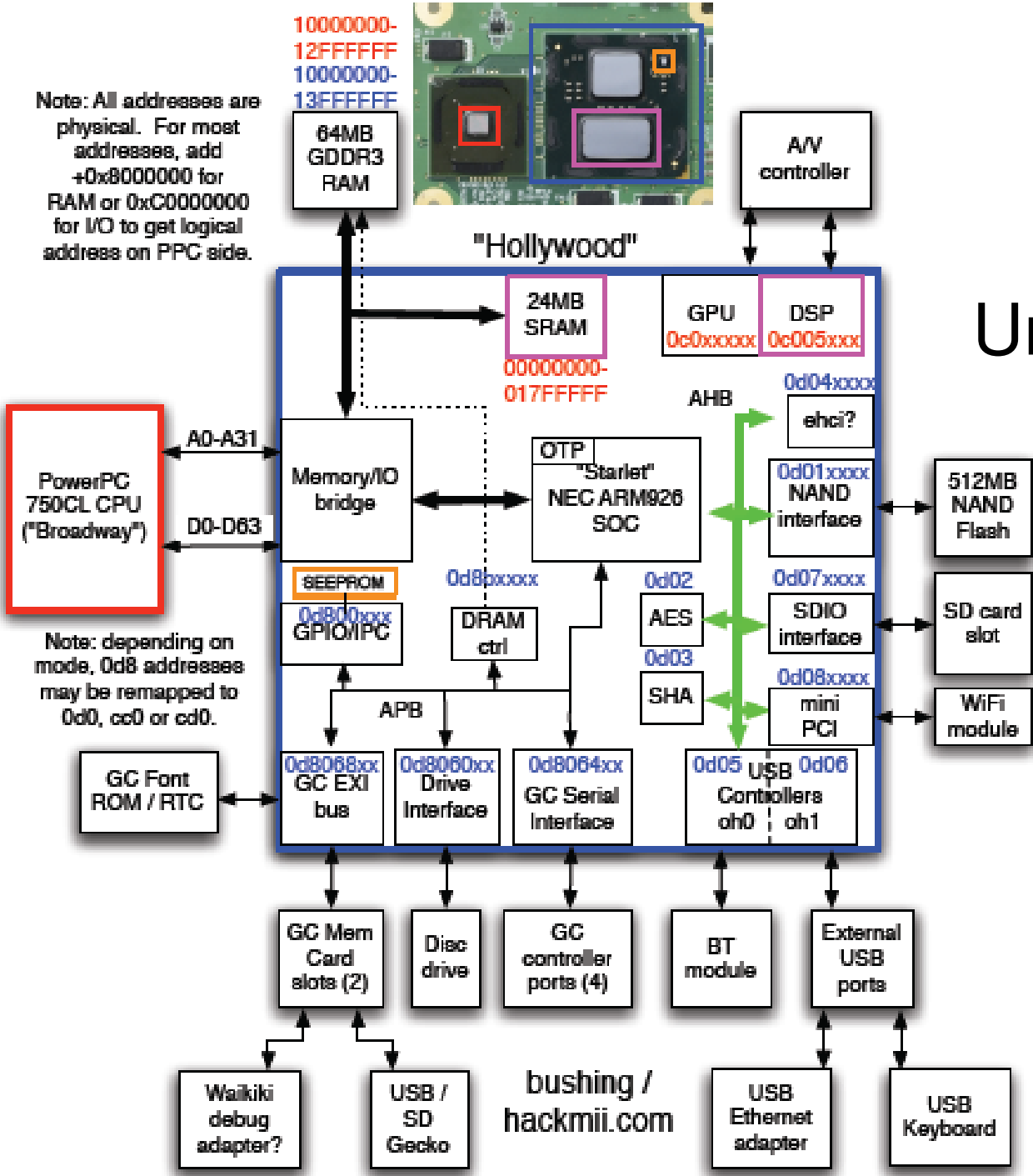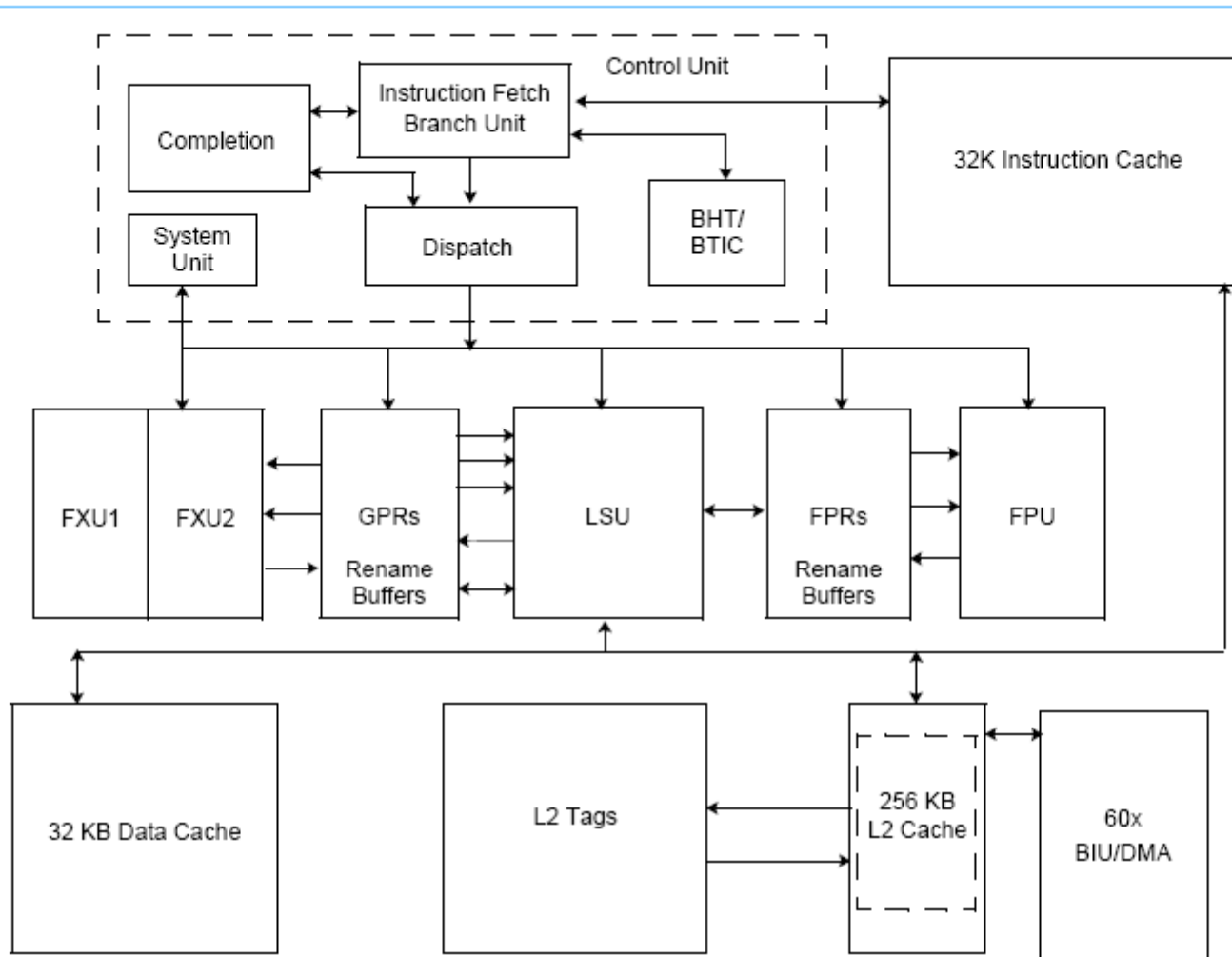
USB Keyboard

.mii.com/wii_hw_diagram.pdf

Table 2-1. PowerPC 750CL Microprocessor Block Diagram

BHT   Branch history table
BIU   Bus interface unit
BTIC   Branch target instruction cache
DMA   Direct memory access
FPR   Floating-point register
FPU   Floating-point unit
FXU   Fixed-point unit
GPR   General purpose register
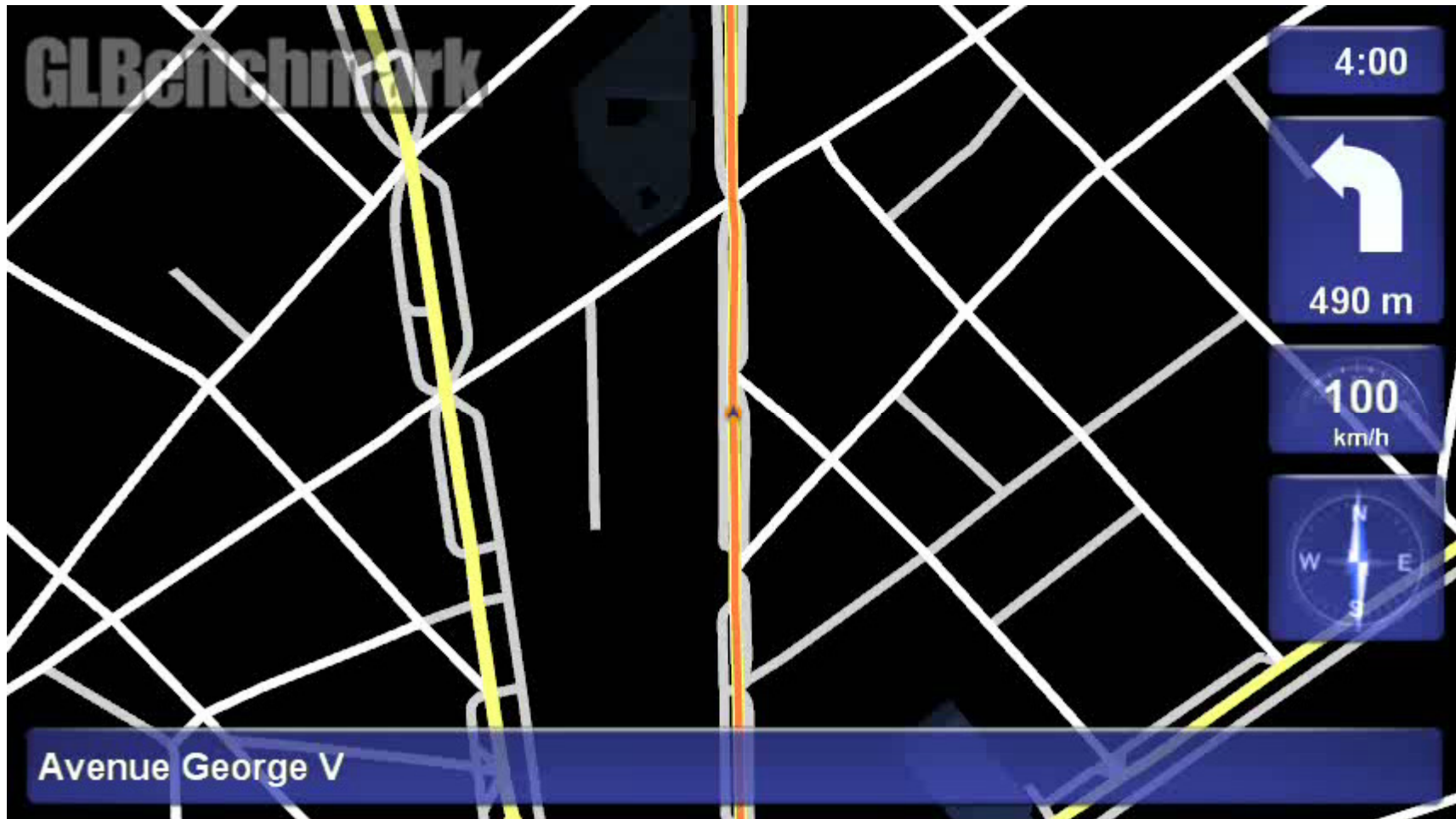L2   Level 2
LSU   Load/store unit

PowerPC 750CL

- Fetch: four instructions per clock
  - Process one branch per cycle
  - 512-entry branch history table
- Dispatch:
  - 2 instructions
- Load/store unit
  - Store gathering
  - Single cycle load/store
  - 32KB L1 cache 256KB L2 cache

Mobile 3D Graphics Benchmarks

Announcements

- Design review:
  - Brining all our designs
  - Ready to explain your design
- Friday (Report Due)
- Final exam: comprehensive (Wed 8:00 AM)
- Course-Instructor Opinion Survey(CIOS)